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CONTENTS

LOW DIELECTRIC CONSTANT NEW MATERIALS FOR MULTILAYER CERAMIC SUBSTRATE

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ABSTRACT

VLSI package development continuously demands new packaging technology to accommodate high signal transmission speed, high wiring density and high frequency pulse requirements for a substrate. Especially for the high signal transmission speed requirement, it is necessary to develop a low dielectric constant material.

Therefore, a low dielectric constant new glass-ceramic material system was developed, whose thermal expansion coefficient and flexural strength could be improved. This material system consists of quartz glass, cordierite and borosilicate glass. The advantages are summarized in the following.

(1)This material system can be sintered at below 1000°C ,so it is possible to use low electrical resistivity conductors, for example, Au, Ag, Ag-Pd and Cu as signal lines and interconnections.

(2)The low dielectric constant can be realized in the 3.9 to 4.7 range.

(3)The thermal expansion coefficient can be controlled to match that for the carried chips.

(4)The flexural strength (2000 kg/cm^2) is relatively high.

By using the green sheet lamination technology, this low dielectric constant multilayer glass-ceramic substrate with Ag-Pd wiring was developed , which can be applied to the high speed VLSI multi-chip packaging substrate.

INTRODUCTION

Recently multilayer ceramic substrates have been developed for VLSI packaging. Due to the increase in switching speed and circuit density in VLSI chips, higher signal transmission speed and wiring densities are required for a multi-chip substrate. In order to accommodate the high wiring density requirement, a low firing temperature multilayer glass-ceramic substrate with Au and Ag-Pd wiring has already been realized.[1] On the contrary, for the high signal transmission speed requirement, it is necessary to develop a low dielectric constant material, because propagation delay time depends a great deal upon the dielectric constant of a substrate.

So low dielectric constant glass-ceramic materials have been developed.[2] These materials are composed of quartz glass /borosilicate glass(BSG)-1 and cordierite/BSG-2, which can be sintered at around 900°C. Dielectric constants are 3.9 and 5.0, respectively, at 1MHz. As a result of investigation on basic pulse transmission properties for various multilayer configurations, it was realized that the propagation delay time decreases due to a lower dielectric constant for the substrate.

Besides, as an important property for the packaging substrate except the dielectric constant, the thermal expansion coefficient(TEC) must be considered. Increases in wiring density require direct bonding of the large chip carrier to the substrate. If TEC is not compatible, the semiconductor will be damaged by the thermal stress. It is desired that TEC for the substrate be as close to that for the chips as possible. However,TEC for quartz glass/BSG-1 is very low (15×10^{-7}/°C) because of quartz glass. On the contrary, TEC for cordierite/BSG-2 is very high (72×10^{-7}/°C) because cristobalite is formed by the crystallization of BSG-2.[3] It is necessary to improve these low dielectric constant materials towards the optimum TEC.

Also the flexural strength is an important factor for the packaging substrate. Fabrication and assembly processes for the VLSI package demand the development of a substrate material whose strength is as high as possible.

This paper describes the low dielectric constant new glass-ceramic material system , whose TEC and flexural strength are improved. This multilayer ceramic substrate, with Ag-Pd wiring, was achieved by using the green sheet lamination technology.

MATERIALS AND PROCESS

The low dielectric constant new glass-ceramic material system consists of quartz glass, cordierite and BSG-1. The original powder, the composition and the particle size distribution have a great influence upon the substrate properties. BSG-1 has low dielectric constant,but doesn't crystallize when SiO_2 and B_2O_3 contents are controlled appropriately. The composition of the quartz glass/ cordierite/BSG-1 composites is shown in Fig.1. Each powder is ground in a ball mill to control the optimum particle size distribution.

A slurry, consisting of the mixed powders and vehicles, was cast into green sheets by a conventional slip casting process. The green sheets were laminated together by press machine. These press conditions are important to control substrate shrinkage and flatness. After the organic binder burn out, sintering was performed at the optimum temperature in air.

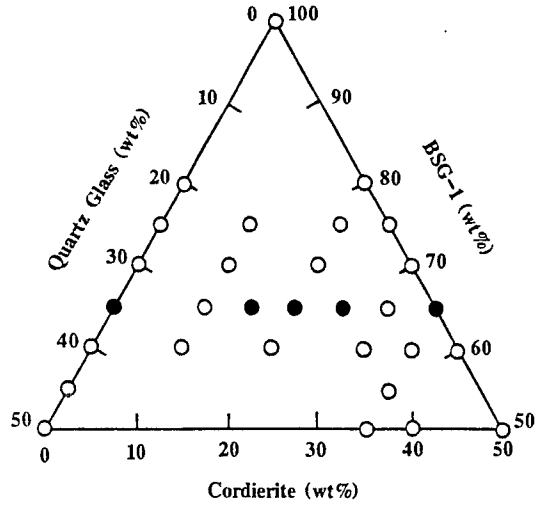


Fig.1 Quartz glass / cordierite / BSG-1 composite composition

RESULTS AND DISCUSSIONS

BSG-1 Content Effect on Sinterability

At first, to set the optimum BSG-1 content in the quartz glass / cordierite /BSG-1 composite, the composites sinterability was examined.

Figure 2 shows the relationship between sintering temperature and BSG-1 content. The sintering temperature is defined as the temperature at which the bulk density agrees with the apparent density, that is, at which open pores become extinct. The sintering temperature for the composites has a specific relation with BSG-1 content, regardless of quartz glass /cordierite content ratio. Therefore, the sinterability is chiefly influenced by the softening fluid property of glass. In case no crystallization occurs in glass which is added as a sintering aid, the softening fluid property is mainly determined by the softening temperature, the particle size distribution and the content in the composite.

The composite microstructure was in more detail observed using SEM. Typical photographs of the polished surface are shown in Fig.3. Figure 3(A),(B) and (C) represent the microstructure for the composite prepared under the conditions below the line, on the line and above the line, respectively, in Fig.2. In Fig.3(A), incomplete softening fluid property of glasses causes the open pores to remain. As seen in Fig.3(B), open pores become extinct. As Fig.3(C) indicates ,very few closed pore remain. The open pores existence is deleterious to reliability for the substrate material. So, it is necessary to accept the conditions existing in the regions above or on the line in Fig.2. Considering the necessity that the composites must be sintered at around 950°C , the optimum BSG-1 content in the quartz glass, cordierite and BSG-1 composite has been fixed at 65 wt%.

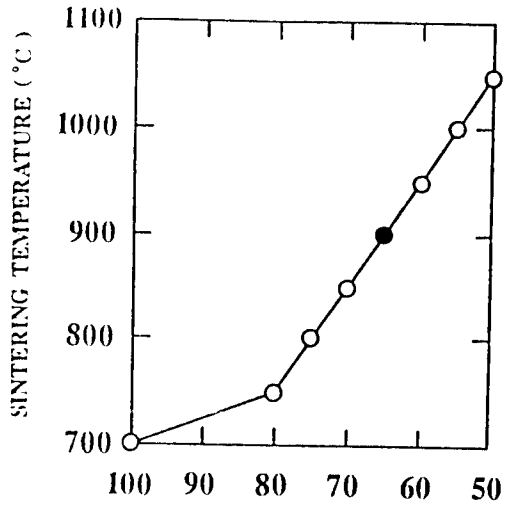
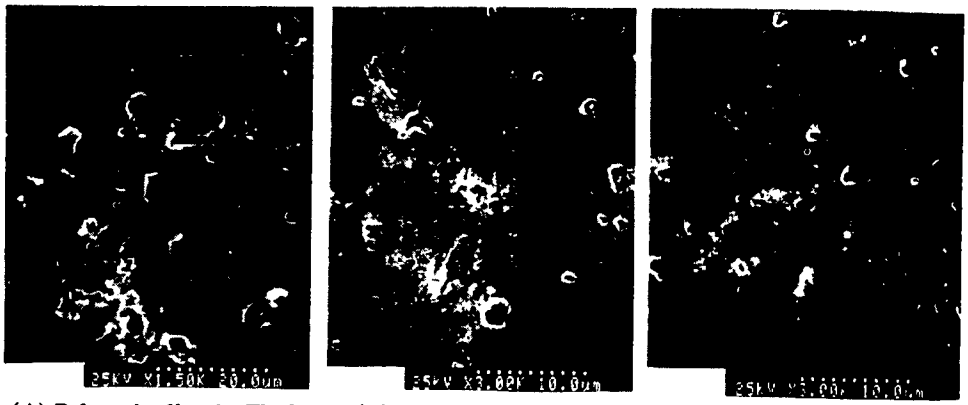


Fig.2 Relationship between sintering temperature and BSG-1 content



(A) Below the line in Fig.2 (B) On the line in Fig.2 (C) Above the line in Fig.2

Fig.3 SEM photographs of polished quartz glass / cordierite / BSG-1 composite surface

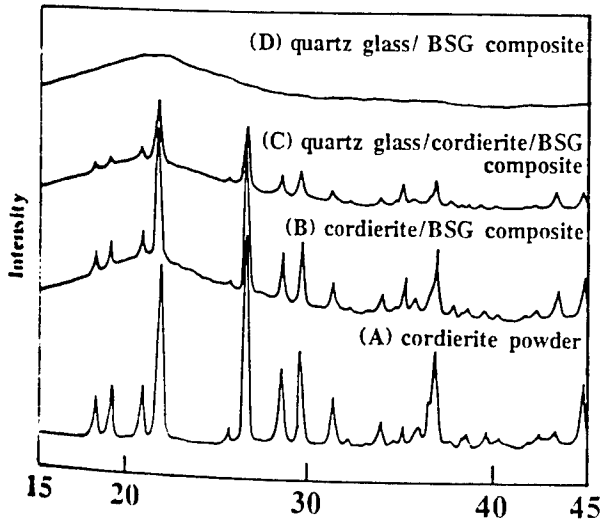


Fig.4 XRD patterns for cordierite powder and the sintered body of quartz glass / cordierite / BSG-1 composites

Quartz Glass/Cordierite Content Ratio Effect on Typical Substrate Properties

Next, to set the optimum quartz glass/cordierite content ratio in the composite, the dependence of each substrate property on the cordierite content was examined. Before describing these results, consider the X-ray diffraction(XRD) patterns for cordierite powder and the sintered body of the quartz glass, cordierite and BSG-1 composites, as shown in Fig.4. Taking into consideration that there are no diffraction peaks, except for cordierite, in the sintered body, there is no cristobalite formation by SiO_2 crystallization and precipitation of a new compound by the reaction between components in the composite. Consequently, it is estimated that the composite has a very simple mixing state.

(1)Thermal Expansion Coefficient

Figure 5 shows the relationship between average thermal expansion coefficient(TEC) (R.T.~250°C) and cordierite content. As mentioned above, the BSG-1 content is constant at 65wt%. So, the cordierite content can be variable from 0 to 35wt% and the remainder is quartz glass. TEC for the composite can be controlled in the 15 to 45×10^{-7}/°C range, depending on the quartz glass/cordierite content ratio. Accordingly, almost the same TEC as that for silicon chips could be realized by a composite containing around 20 wt% of cordierite and 15 wt% of quartz glass.

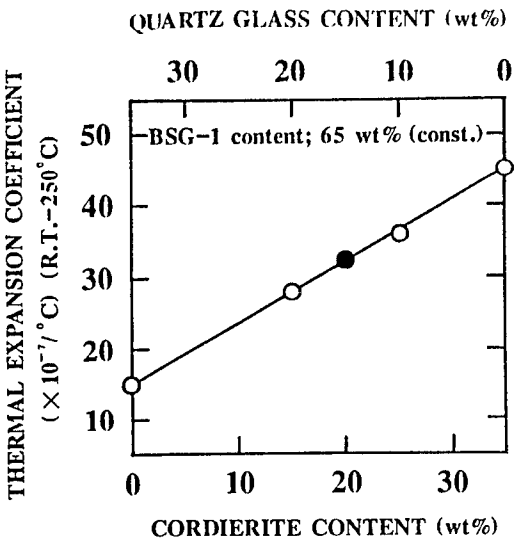


Fig.5 Relationship between thermal expansion coefficient and cordierite content

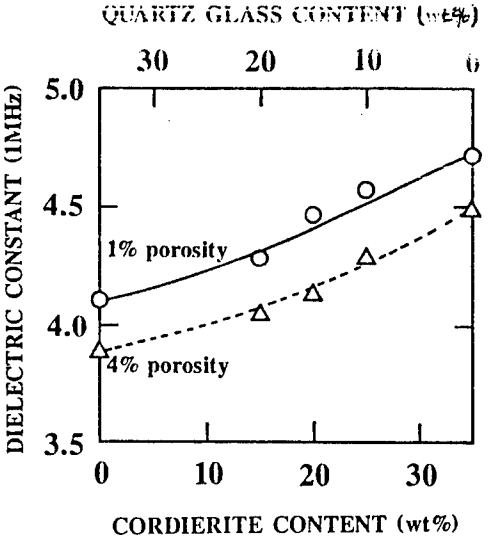


Fig.6 Relationship between dielectric constant and cordierite content

(2)Dielectric Constant

Figure 6 shows the relationship between dielectric constant(1MHz) and the cordierite content. The solid line indicates that the composites fired at 950°C have 1% closed porosity, that is, very dense microstructure, while the broken line indicates that 4% closed porosity is introduced into the sintered body of the composites fired at 900°C. It is well known that the introduction of pores is very effective to lower dielectric constant.[4] Figure 7 shows the relationship between dielectric constant and porosity for the quartz glass/BSG-1 composite. These measured values are in fair agreement with Lichtenecker's mixing rule. By controlling various conventional fabrication conditions, for example, firing condition, about 4% closed porosity can be introduced, as a maximum. However, over this porosity value, open pores unexpectedly form in addition to closed pores. As mentioned above, the formation of open pores is undesirable for the substrate material. Consequently, determining how pores are isolated is an important point in reducing the dielectric constant. At present, the dielectric constant for the composite can be controlled in the 3.9 to 4.7 range, depending on the quartz glass/cordierite content ratio and the controlled porosity.

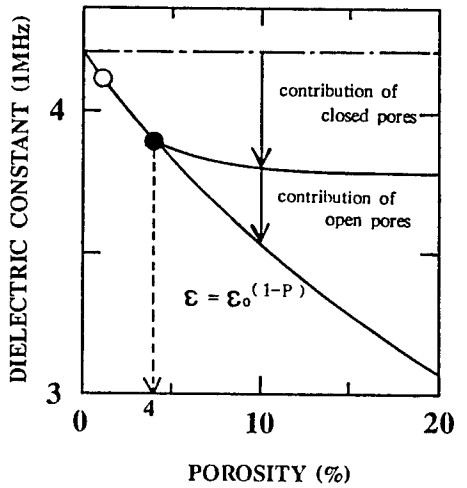


Fig.7 Relationship between dielectric constant and porosity for the quartz glass / BSG-1 composite

(3)Flexural Strength

Figure 8 shows the relationship between flexural strength and cordierite content. The presently reported glass-ceramic composites have a homogeneous structure with evenly dispersed ceramic particles in the glass matrix. Dispersed ceramic particles make a contribution to restrain the size of Griffith crack[5] and promote the propagation energy of cracks, so the mechanical properties for the glass-ceramic composite are improved in comparison with simple glass. Moreover, an effective method to better the mechanical properties involves controlling dispersed particle size and must be considered. Generally, a decrease in particle size causes a reduction in the maximum crack length, that is, it causes a decided improvement in the flexural strength for ceramic materials.[6] The results indicated by the broken line in Fig.6 can be obtained by using finer grinding powder than usual. On the contrary, an increase in the cordierite content in the composite brings about an improvement in the flexural strength. Especially, the cordierite/BSG-1 composite has 2000 kg/cm^2, which is sufficient for practical use as a substrate material.

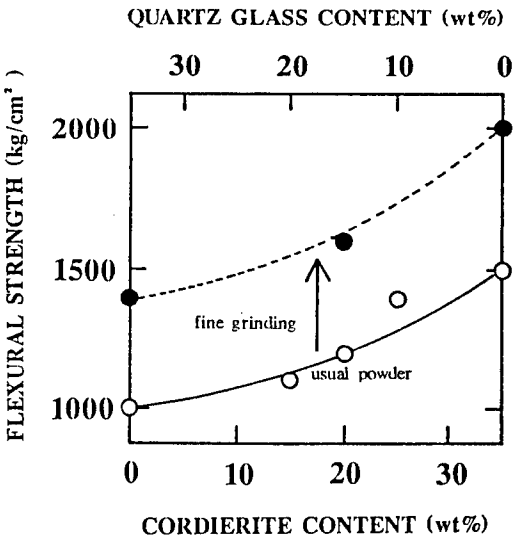


Fig.8 Relationship between flexural strength and cordierite content

New Multilayer Glass-Ceramic Substrate with Low Dielectric Constant

As a result of the above investigation, three kind of low dielectric constant new materials were applied to multilayer glass-ceramic(MGC) substrates. Typical properties for these substrates are summarized in Table 1. Individual substrates have the following outstanding characteristic.

(1) MGC substrate, composed of 35wt% quartz glass and BSG-1, has an extremely low dielectric constant(4.1), even if its microstructure is very dense. Moreover, due to the introduction of controlled porosity into its microstructure, that value can be lowered to 3.9.

(2) On the contrary, MGC substrate, composed of 35wt% cordierite and BSG-1, has a relatively high flexural strength (2000 kg/cm^2) due to uniform dispersion of finer ceramic particles in the glass matrix.

(3) MGC substrate composed of 15wt% quartz glass, 20wt% cordierite and BSG-1 has almost the same thermal expansion coefficient(32×10^{-7}/°C) as Si chips. Besides, both dielectric constant(4.4) and flexural strength (1600 kg/cm^2) are the average value, compared with the other two MGC substrates.

There is no difference in sinterability between these substrates, because of the constant BSG-1 content. So, sintering temperature is invariably 900°C and the relative density can be promoted to more than 99% by appropriate control of glass particle size distribution and the firing condition.

The dielectric properties, except dielectric constant, in other words, the dissipation factor and insulation resistance are also favorable, 0.2% and $>10^{14}$ohm·cm, respectively. There is no dielectric constant and dissipation factor dependence in the 1kHz to 10MHz frequency range for every MGC substrate. Shrinkage tolerance and flatness for the new MGC substrates can be controlled at the same level as that for the conventional MGC substrate.

Furthermore, the low dielectric constant new MGC substrates, which are fabricated by co-firing up to 33 Ag-Pd metallized layers, can be realized on that test pattern. Figure 9 shows the external appearance of a typical new MGC substrate composed of 15wt% quartz glass, 20wt% cordierite and BSG-1. The size is 100×100mm.

CONCLUSION

Low dielectric constant new MGC substrates, composed of quartz glass, cordierite and borosilicate glass, where cristobalite crystallization doesn't occur, have been developed by green sheet lamination technology. This material system has the following excellent characteristics.

(1) A reduction in the processing temperature to below 1000°C facilitates the utilization of low electrical resistivity conductors.

(2) The low dielectric constant can be realized in the 3.9 to 4.7 range. The propagation delay time can be reduced by more than 30%, comparable to the alumina substrate.

(3) Almost the same thermal expansion coefficient as that for Si chips makes it possible to mount the large size chip carriers on the package directly.

(4) Relatively high flexural strength and favorable dielectric property improve the substrate material reliability and allow practical use for VLSI packages.

(5) High density packaging and accurate shrinkage control can be realized by a conventional fabrication process.

In the future, this low dielectric constant new multilayer glass-ceramic substrate with Ag-Pd wiring will be applied to the high-speed VLSI packaging substrate in a large scale computer system.

ACKNOWLEDGMENT

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Table 1 Typical Low Dielectric Constant MGC Substrate Properties

Substrate Property	Quartz Glass / BSG	Quartz Glass / Cordierite / BSG	Cordierite / BSG
Sintering Temperature (°C)	900	900	900
Sintered Density (g/cm^3)	2.17	2.24	2.33
Dielectric Constant (1MHz)	4.1	4.4	4.7
Dissipation Factor (1MHz)	0.002	0.002	0.002
Insulation Resistance (Ω cm) (50V D.C.)	$>10^{14}$	$>10^{14}$	$>10^{14}$
Thermal Expansion Coefficient ($\times10^{-7}$/°C)	15	32	45
Flexural Strength (kg/cm^2)	1400	1600	2000
Linear Shrinkage (%)	13.9	14.6	15.7
Shrinkage Tolerance (%)	< 0.3	< 0.3	< 0.3
Camber (μm/100mm)	40	20	20
Roughness (μm Ra)	0.5	0.4	0.4

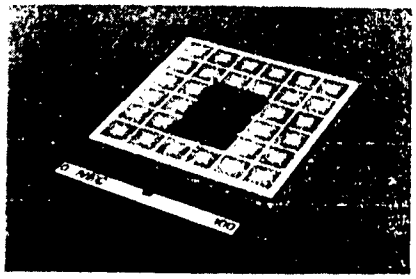

Fig.9 Typical new MGC substrate

Co-fireable Copper Multilayered Ceramic Substrates

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ABSTRACT

This paper discusses the manufacture of co-fireable Copper Multilayered Ceramic Substrates utilizing green tape technology. It includes the results of our development substrate materials and a new manufacturing process for the Copper Multilayered Ceramic Substrates using CuO paste as a conductor. Also discussed are the excellent properties and a superiority of our development.

INTRODUCTION

As a way to realize high density circuit boards, we developed the Copper Multilayered Ceramic Substrates and established a new original manufacturing process. This process is most similar to the MLC processes except that the copper oxide paste is used as a conductor, that the burnout process is performed in the air, the reduction process is carried out in the nitrogen atmosphere containing 10% hydrogen in which copper oxide is reduced into copper, and sintering is performed in the nitrogen.

We developed two types substrate materials, the one is a crystallizable glass which has a strong flexural strength, another one is an amorphous glass which has a low dielectric constant. Combing this new process with these substrate materials, we succeeded in developping the Copper Multilayered Ceramic Substrates which has excellent properties and high reliability.

THEORETICAL

In our manufacturing process, the most particular point is using a oxidation-reduction reaction. The calculation was carried out to lead the temperature at which CuO is reduced to Cu in the reduction process from the view point of Gibbs' free energy.

$$CuO + H_2 \rightarrow Cu + H_2O \qquad \Delta G$$

If ΔG is negative at a particular temperature, CuO can be reduced to Cu in a hydrogen atmosphere, so ΔG was calculated by the material [1], the value is nearly egual to −24 kcal at 25℃. this result means that reduction reaction can advance at even a room temperature theoretically. But this calculation is not taken into consideration of the rate of reaction and is assumed infinite reaction. As a result, useful data can not be available theoretically from this calculation.

Secondly, differential thermal analysis was carried out with CuO powder, the average grain size of which was 0.03 μm and 3.0 μm, in a nitrogen atmosphere containing 10% hydrogen. These results are shown in Table 1. The results of this analysis indicate that the reduction reaction from CuO to Cu is exothermic reaction and that the peak temperature of reduction are 220℃ for 0.03 μm CuO powder and 300℃ for 3.0 μm CuO powder.

Table 1 DTA Analysis of CuO Powder

Average Diameter of CuO Powder	Exothermic Peak Temperature
0.03 μm	220 ℃
3.0 μm	300 ℃

EXPERIMENTAL

MATERIALS

(1) Substrate Material

Among the performances required of substrate material are fireable in a nitrogen atmosphere at 900℃, excellent mechanical and electrical properties. The firing temperature is preferable to be below the melting point of conductor materials, because breaking circuit and deformation of signal pattern should occur for firing over the melting point of conductor. The firing temperature of substrate was decided at 900℃ so that the melting point of Cu is 1083 ℃ and moreover potential of the multilayer substrates with interlayered resistors and capacitors is expected. [2] [3] [4] Two types of ceramic compositions are shown in Table 2, and a photograph of their co-firing with inner layer conductors is shown in Fig. 1.

Table 2
Ceramic Composition for Substrate Materials

Component		A	B
Glass	SiO_2	27	28.8
	Al_2O_3	−	10.8
	B_2O_3	2.7	0.6
	Na_2O	1.4	−
	K_2O	0.9	0.6
	CaO	3.6	4.8
	MgO	1.4	1.8
	BaO	−	3.6
	PbO	8	9
Alumina		55	40
Total		100	100

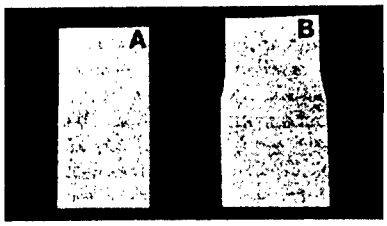

Fig. 1 Deformed substrate photograph by Ceramic composition difference

Fig. 1 reveals that substrate of type B has been deformed, while type A has no deformation. Thus the adaptability of substrate and inner layer conductor is greatly influenced by ceramic composition of substrate. [5] We developed characteristic two types ceramic compositions . The one is a crystallizable glass, we called MKE − 1 0 0, which has a strong flexural strength, its main crystalline phase is 0 . 3 5 $NaAlSi_3O_8$ − 0 . 6 5 $CaAl_2Si_2O_8$ (labradorite) and a solid solution of both $NaAlSi_3O_8$ (albite) and $CaAl_2Si_2O_8$ (anorthite) . Another one is an amorphous glass, we called MKE − 2 0 0, which has a low dielectric constant and has a thermal expansion coefficient near Si.

(2) Vehicle

Vehicle is used to form the ceramic powder into green tapes. The needs for vehicles are the green tape casting without cracks, uniform ceramic powder dispersion, good lamination property, the low thermal decomposition temperature. These characteristics are affected by the molecular weight, acid value, Tg, molecular structure of the polymer respectively.

The thermal decomposition is expected by the bond-dissociation energy between the two elements of each molecule. It is shown in Table 3.

Table 3 Bond-Dissociation Energy

Molecular Structure	Bond-Dissociation Energy	
$H_3C - \overset{\downarrow}{C}H_2CH=CH_2$	310	KJmol^{-1}
$H_3C - CH_2\dot{C}H=CH$	134	KJmol^{-1}
$H_3C - CH_3$	368	KJmol^{-1}
$H_3C - CH_3$	402	KJmol^{-1}

Table 3. gives that the molecules with acrylic acid structure have the small bond-dissociation energy, because the electrons which participate in the binding of the corbon which is located at the end of the allyl-radical ($-CH-CH=CH_2$) to its first neighbor carbon are pulled into the allyl radical by the allyl resonance, so that the bond-dissociation energy is decreased. [6] The acrylic resin has the low Tg generally and the convenient property of thermal decomposition by above discussion. So, we use a copolymer of methyl-acrylate, ethyl acrylate and ethyl methacrylate as a binder, methyl ethyl keton as a solvent, and buthyl benzil phthalate as a plasticizer.

(3) CuO paste

The CuO paste developed as an inner layer conductor is made up of 3 . 0 μm CuO powder, glass frit having a softening point of 6 0 0 ℃, acrylic resin, buthyl calbitol acetate, terpineol and additives. As mentioned before, 3 . 0 μm CuO powder is reduced to copper at 3 0 0 ℃ in a nitrogen atmosphere containing 1 0 % hydrogen.

To decide the industrial reduction condition, we made the following experiments. The laminated green tapes with CuO inner layer conductor were pre-fired in a convection oven at 5 5 0 ℃ in air, next reduced under the condition which the reduction peak time is 2 0 min, the reduction peak temperature is changed from 2 5 0 ℃ to 4 5 0 ℃ in a nitrogen atmosphere containing 1 0 % hydrogen, and fired at 9 0 0 ℃ in a nitrogen atmosphere. Then the sheet resistance of the inner layer conductor was measured, the results is shown in Fig. 2. As revealed by the figures, the sheet resistance proves to stabilize when copper oxide is reduced at just a little under 3 0 0 ℃ or higher. Thus, the temperature in the reduction process has been determined as 3 5 0 ℃.

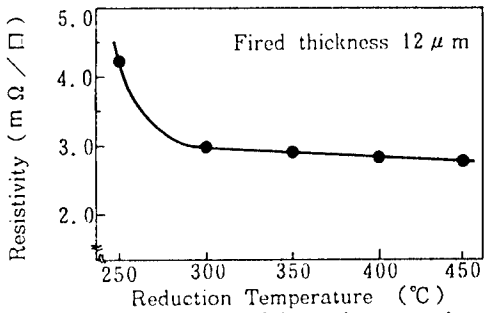

Fig. 2 Sheet resistance of inner layer conductors by reduction temperature

(4) Cu paste

Commercial Cu paste is used as the top layer conductor.

PROCESS

Our development Copper Multilayered Ceramic Substrates are manufactured by the process shown in Fig . 3

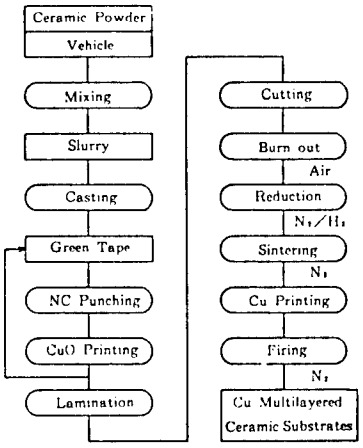

Fig. 3 Flow Chart for Copper Multilayered Ceramic Substrates Processing

The ceramic powder and the vehicle are mixed by ball-milling, a slurry consisting of these materials is cast into thin ceramic green tapes by a conventional doctor blading method, via holes are formed through the green tape using NC punching equipment. Via holes are filled with CuO paste to form contact between signal lines or electrode, and CuO paste is applied as an inner layer conductor. These printed green tapes are laminated together at 8 0 ℃ under a pressure of about 2 0 0 kg / cm^2. These laminated green tapes are pre-fired at 5 5 0 ℃ in air, reduced at 3 5 0 ℃ in a nitrogen atmosphere containing 1 0 % hydrogen in which CuO is reduced to Cu and co-fired at 9 0 0 ℃ in a nitrogen atmosphere. Fig. 4. shows the temperature and atmospheric profile of these firing processe.

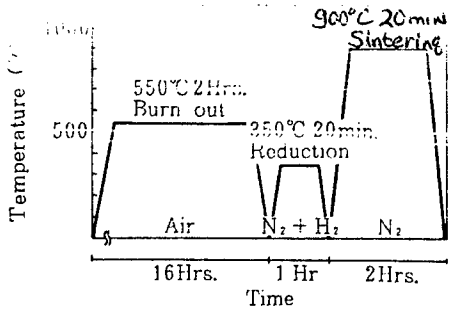

Fig. 4 Temperature and Atmospheric Profile of Firing Process

The reason we choosed a nitrogen atmosphere containing 10% hydrogen as a reduction atmosphere is extremly safety, shown in Fig. 5, from the view point of explosive limits. [7]

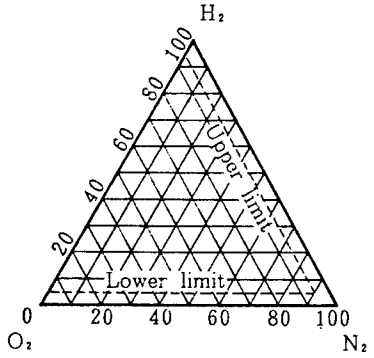

Fig. 5 Explosive limits of H_2-O_2-N_2 system

Fig. 6 shows SEM photographs of the inner layer surfaces during processes. Fig. 7 shows SEM photographs of the substrate sections during processes.

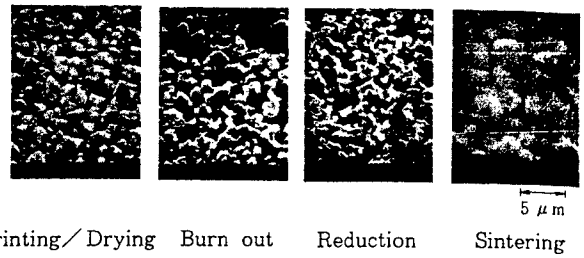

Fig. 6 SEM Photographs of Inner Layer Conductor Surfaces During Processes

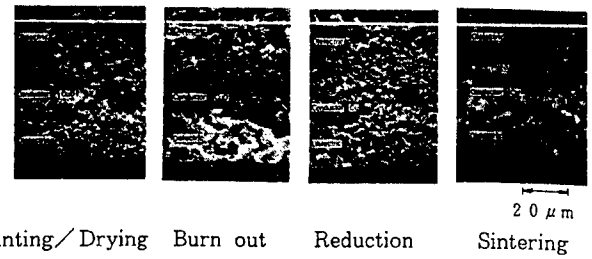

Fig. 7 SEM Photographs of Substrates Sections During Processes

Finally, the [illegible] Cu paste as a top layer conductor is applied by screen printing, and fired at 900℃ in a nitrogen atmosphere employing conventional belt furnace.

RESULTS

The excellent properties of our development copper multilayered ceramic substrates, obtained from utilizing these technologies are shown in Table 4 and Table 5.

Table 4 Properties of Copper Multilayered Ceramic Substrates

Properties		MKE−100
Sintered density	(g/cm³)	3.1
Flexural strength	(kg/cm²)	2500
Thermal expansion coefficient	(℃⁻¹)	61.2×10^{-7}
Dielectric strength	(KV/mm)	>15
Volume resistivity	(Ω・cm)	$>10^{14}$
Dielectric constant	(1 MHz)	7.4
Dissipation factor	(1 MHz)	0.002
Thermal conductivity (cal/deg・cm・sec)		0.007
Conductor sheet resistance	Inner	3
(mΩ/□)	Top	2

Table 5 Properties of Copper Multilayered Ceramic Substrates

Properties		MKE−200
Sintered density	(g/cm³)	2.5
Flexural strength	(kg/cm²)	1400
Thermal expansion coefficient	(℃⁻¹)	42.0×10^{-7}
Dielectric strength	(KV/mm)	>15
Volume resistivity	(Ω・cm)	$>10^{14}$
Dielectric constant	(1 MHz)	4.5
Dissipation factor	(1 MHz)	0.002
Thermal conductivity (cal/deg・cm・sec)		0.007
Conductor sheet resistance	Inner	3
(mΩ/□)	Top	2

CONCLUSION

The establishment of a new manufacturing process of Copper Multilayered Ceramic Substrates using a oxidation-reduction reaction, employing CuO paste as an inner layer conductor, and the development of two types ceramic compositions as an insulating substrate materials has brought about the production of Copper Multilayered Ceramic Substrates having excellent characteristics. The excellent characteristics are as follows.

(1) The superiority of low impedance, migration resistance and low cost has resulted from Cu conductor.

(2) The burnout process permits the use of air, organic components are removed completely. This results in excellent insulation performance and high reliability for the substrates.

(3) The development of substrate materials, MKE − 1 0 0 which has a strong flexural strength 2 5 0 0 kg / cm² and a low dielectric constant 7 . 4 (1MHz) less than Al_2O_3, and MKE − 2 0 0 which has a low dielectric constant 4 . 5 (1MHz) and the nearly thermal expansion coefficient $4 . 2 \times 10^{-6}$ ℃$^{-1}$ as Si, makes us to be able to respond to broad demands.

We are convinced that as a result of our development can be put into practical application, and that such substrates could come into broad use for consumer electronic products in the near future.

ACKNOWLEGEMENTS

The authors would like to thank S. Amano, the managing director of Matsushita-Kotobuki Electronics Ind., Ltd. and Dr. M. Nagasawa, the director of Development Research Laboratory, Matsushita Electric Industrial Co., Ltd. for their valuable discussions and encouragement.

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YTTRIA STABILIZED ZIRCONIA THIN FILM PREPARED BY RF MAGNETRON SPUTTERING METHOD

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〈ABSTRACT〉

Yttria stabilized zirconia (YSZ) thin films were obtained by means of R.F. magnetron sputtering using sintered YSZ targets. Three types of targets were used in order to investigate the effect of the amount of Y_2O_3. These contain 3, 9 and 20 mol% Y_2O_3 as the stabilizer.

Preparation conditions, physical and electrical properties were examined by X-ray diffraction analysis, I-V measurement of MOS structure which was fabricated by evaporating Al electrode on YSZ film on Si, and photoabsorption characteristics. Crystallinity of the sputtered layer depended on the substrate temperature. As the substrate temperature was above 300 [℃], polycrystalline YSZ film was obtained. The phase of film was dominated by the amount of doped Y_2O_3 in the target. Dielectric constant and optical energy gap was found to be 24.5~28.6 and ~4.4 [eV], respectively.

(YSZ:yttria stabilized zirconia) has been studied by many workers. Y.Miyahara[2] used YSZ as a sensitive part of oxygen sensor. And H.Myoren[3] used ZrO_2 as buffer layer between the superconducting oxide material and Si(100) substrate. It is desirable to prepare thin film of stabilized zirconia in order to apply to electronic devices described above. However, there are not so many reports about zirconia thin films and the effect of doping on properties of zirconia thin films. Because the studies on the application for electronic devices and high fracture strength thin film materials have only started just recently.

In this report, the formations of yttria stabilized zirconia (YSZ) thin films were investigated and the effects of Y_2O_3 doping on zirconia thin films were examined by X-ray diffraction analysis, I-V measurement of MOS structure, photoabsorption characteristics. YSZ films were applied to buffer layer and oxygen sensor.

Using this YSZ film as a buffer layer on alumina substrate, the superconducting properties of Y-Ba-Cu-O was observed. Gas sensitive properties of the films were also confirmed.

INTRODUCTION

Zirconia ceramics (ZrO_2) is becoming one of the most promising high fracture strength and toughness materials. Pure ZrO_2 exhibits three polymorphs, i.e. monoclinic(M), tetragonal(T) and cubic(C). The tetragonal-monoclinic transformation of ZrO_2 changes the volume. This change causes fracture itself. Divalent or trivalent metal oxide (such as CaO, Y_2O_3, etc.) has been used as dopant to protect from fracture[1]. It has been known that the doping improve the characteristics of zirconia ceramics.

Recently zirconia doped with Y_2O_3

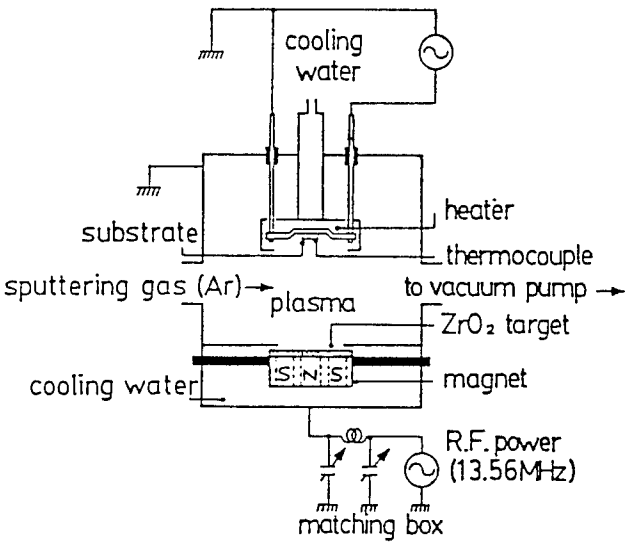

Fig.1 The schematic of experimental apparatus.

EXPERIMENT

YSZ thin films were deposited on Si(100), vycor glass and ceramics (poly-Al_2O_3) substrates by means of R.F. magnetron sputtering using sintered targets. Three types of targets were used in order to examine the effects of Y_2O_3. These contain 3, 9 and 20 mol% Y_2O_3 as the stabilizer.

Figure 1 shows a schematic diagram of the apparatus. Sputtering conditions for preparing thin films are shown in Table] . The system evaporation was evacuated by conventional oil diffusion pump. The background pressure was lower than $5 * 10^{-4}$ [Torr]. The discharge gas Ar, which was introduced into the chamber through needle valve and flow meter, was used. The substrate was heated to about 750 [℃] by carbon heater.

The relation between film thickness and substrate temperature is shown in Figure 2. As the substrate temperature was elevated, film thickness was increased. Film thickness was decreased with increased the amount of doped Y_2O_3 in the target. The average deposition rate was calculated to be ~ 22[Å/min] when the film was deposited at 700 [℃] using the target with 3 mol% Y_2O_3.

TABLE I Sputtering Conditions of YSZ Thin Films

Substrate	n-Si(100) ρ=8.0~12.0[Ω·cm] p/p⁺Si(100) ρ=13.6[Ω·cm] Vycor Glass Ceramics(poly-Al_2O_3)
Substrate Temp.	R.T.~ 750°C
Deposition Time	180 min. 300 min.
R.F. Power	70 W
Target(ZrO_2:Y_2O_3)	1:3 mol% 1:9 mol% 1:20 mol%
Chamber Pressure	5~10 mTorr
Sputtering Gas	Ar

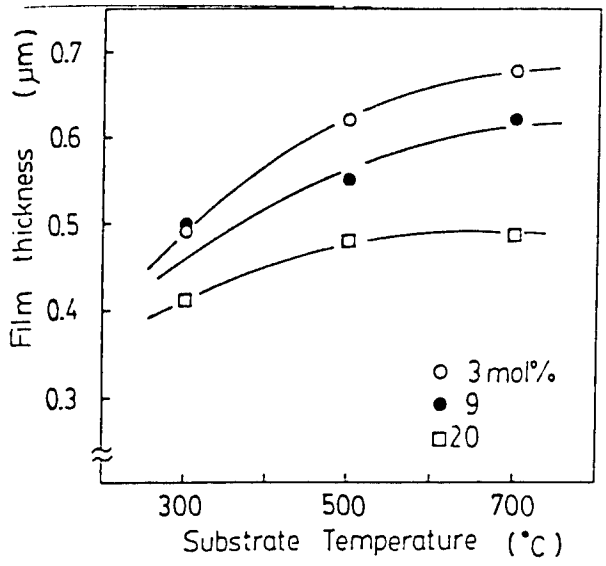

Fig.2 Relation between deposition rate and substrate temperature. (Deposition time was 300 [min].)

the ratio is larger than 1, the film has excess Y compared with the target composition ratio. This result shows that the lower the substrate temperature is or the less the amount of doped Y_2O_3 is, the more the ratio of Y in the film increases. However, the discrepancy can be neglected because the values are almost around 1.

Figure 4 shows the X-ray diffraction patterns of YSZ films. These films were deposited at different substrate temperature using the target with 9 mol% Y_2O_3. As the substrate temperature was above 300 [°C], polycrystalline YSZ film was obtained. The dominant diffraction peak changed from 29.8° to 34.9° as the substrate temperature was increased. In other words, the dominant phase changed to tetragonal phase, mixed (tetragonal+cubic) phase and cubic phase at the substrate temperature was about 300 [°C], 500[°C] and 700[°C], respectively. The phase transitions in films was observed.

It is obvious that Y_2O_3 doping has much effect on the crystal structure. Because tetragonal or cubic phase of pure ZrO_2, which appeared at only high temperature region (above 1100[°C]) was observed. Using the target with 3 mol% Y_2O_3, the different phase transition in YSZ films was observed. In this case, the dominant phase changed to mixed (monoclinic+tetragonal) phase, tetragonal phase and mixed (tetragonal+cubic) phase at the substrate temperature was 300[°C], 500[°C] and 700[°C], respectively. These results show that the phase of film was dominated by the amount of doped Y_2O_3 in the target.

RESULTS AND DISCUSSION

A. Composition and Crystallinity

The film composition was examined by electron prove micro analysis and the crystallographic structure of films by X-ray diffraction analysis.

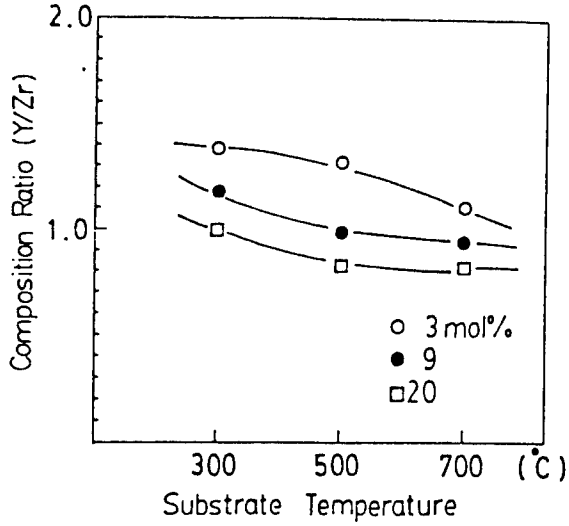

Fig.3 The composition ratio film versus target.

Figure 3 shows the dependence of the composition ratio of the film on substrate temperature. This ratio was compared with the original target composition ratio. In other words, the vertical line shows the discrepancy between the film composition ratio and that of the target. When the ratio is 1, the film has the same composition ratio of the target. When

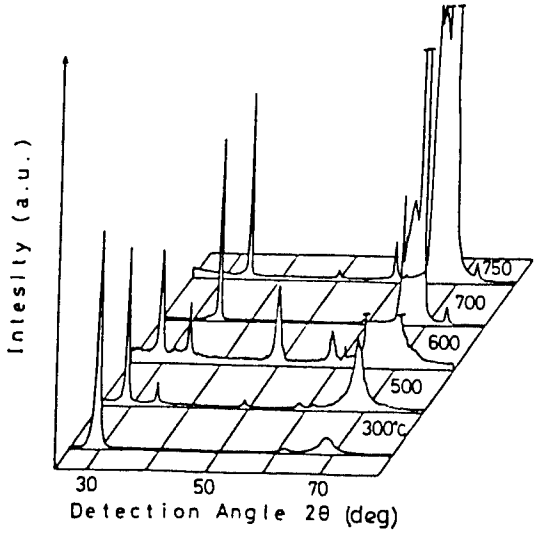

Fig.4 Typical X-ray diffraction patterns depending on the substrate temperature. (using the target with 9 mol% Y_2O_3)

B. Photoabsorption

It is important to make clear the optical properties of YSZ films for application to coating films of optical devices and to determine the energy gap. The transmission factor of YSZ film was measured. The samples were deposited on vycor glass. The optical energy gap was calculated from the photoabsorption characteristics.

Figure 5 shows the characteristics of transmission versus wavelength for the films

deposited at 500 [°C]. Three types target were used. In the visible radiation region which were in the range from 300 to 700 [nm], the transmission factor was above 70 %. The absorption edge was observed at about 250 [nm]. The transmission factor was almost independent of the amount of Y_2O_3 doped ZrO_2.

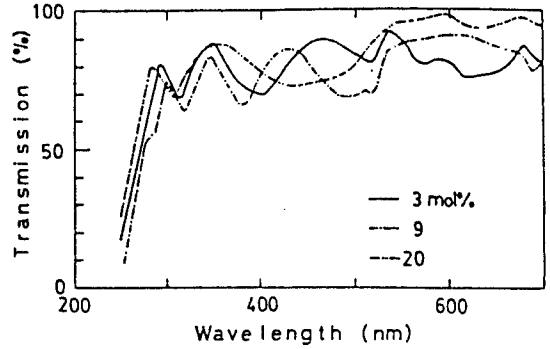

Fig.5 The characteristics of transmission versus wavelength.

The values of optical energy gap calculated from these characteristics are shown in TableII. These values were in the range from 3.86 to 4.40 [eV]. These tended to increase as increasing the amount of Y_2O_3.

C.Electrical characteristics
(I-V measurement)

Figure 6 shows the current-voltage characteristics of MOS structure (Al-YSZ-Si substrate). YSZ films were deposited at room temperature. As in this figure, there are two distinct regions. The currents change

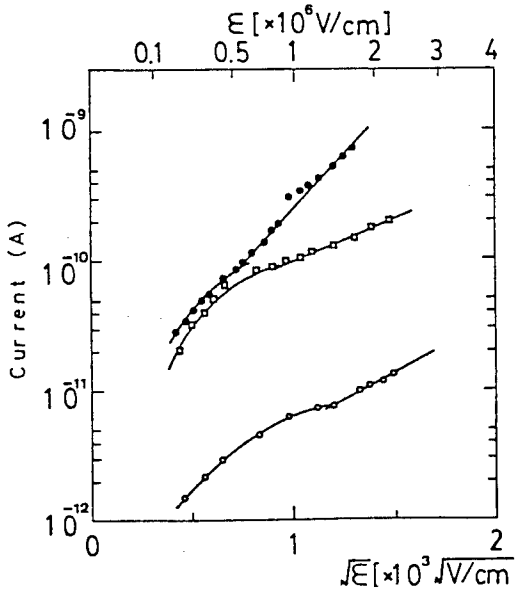

Fig.6 Current versus square root of electric field for Al-YSZ-Si structures at room temperature with an area of $1.257*10^{-3}cm^2$ for aluminum electrode positive.

APPLICATION

A.Buffer layer for high T_c superconductor

As one of applications of the YSZ film, the film was used as buffer layer between Y-Ba-Cu-O film and alumina substrate. The Y-Ba-Cu-O films were prepared by D.C magnetron sputtering apparatus. The target with the atomic ratio of Y:Ba:Cu = 1:3:7 was used. The thickness of Y-Ba-Cu-O film and YSZ layer were about 2~3 [μm] and 0.3 [μm], respectively. After deposition, the samples were annealed in O_2 atmosphere at 850 [°C] for 1 hour. The resistivity was measured by the conventional four-point probe method.

Figure 7 shows the temperature dependence of the resistivity of Y-Ba-Cu-O films with and without YSZ layer. The resistance of the sample with YSZ layer behaved a rapid drop at 95 [K]($T_{c\,ON}$) and zero resistance at 47 [K]($T_{c\,OFF}$). The resistance of the sample without YSZ layer had the negative temperature coefficient and these samples did not indicate zero resistance. From these results, YSZ layer was found to be useful as the buffer layer between the superconducting film and alumina substrate. However, as in this figure, the resistance exhibited a long tail below the $T_{c\,ON}$. It is considered that this result was caused by the growth of second phase (CuO,etc.) in superconducting layer and the crystallinity of YSZ layer was not single crystal completely.

TableII The value of optical energy gap.

	Thickness	Sub.Temp.	The Value of The Band Gap
1:3mol%	175 (nm)	700 (℃)	3.86 (eV)
	171	500	4.16
	159	300	3.93
1:9	135	700	4.06
	270	500	4.23
	200	300	4.40
1:20	100	700	4.25
	150	500	4.33
	150	300	4.31

exponentially with the square root of the field at high electric field, the characteristics are ohmic at low field. As the amount of doped Y_2O_3 was increased, the current value was increased. The resistivity of YSZ films were calculated to be $\sim 2.23 * 10^{13}$ [Ω·cm].
The resistivity of the film obtained using the target with 20 mol% was higher than that of the film using the target with 9 mol% Y_2O_3. Because Y^{3+} couldn't replace Zr^{4+} completely, so Y_2O_3 remained unsubstitutionally in the films. These characteristics were similar to that of Si_3N_4 film as an insulator in MIS structure[4]. However the resistivity of YSZ films were smaller than that of Si_3N_4 film. As the crystallinity of film was improved, the resistivity decreased.

Dielectric constant of films deposited at room temperature was found to be 24.5~28.6. The value of film deposited at 500 [°C] using the target with 9 mol% Y_2O_3 was 68. These value was increased depending on crystallinity of films.

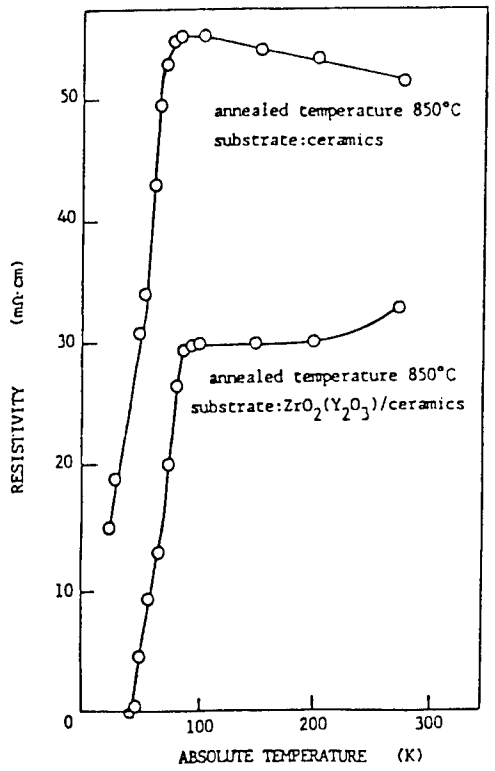

Fig.7 The temperature dependence of the resistivity of the Y-Ba-Cu-O thin films.

B.Gas sensitive properties

Y_2O_3 doped ZrO_2 which is a good oxygen conductor due to presence of oxygen vacancies formed by the doping. Recently, stabilized zirconia has been applied to oxygen sensor using these characteristics. The currents flowing through the surface of the YSZ films were examined dependening on oxygen.

The schematic representation of the experimental setup is shown in Figure 8. The sample was in the chamber evacuated to about 100 [mTorr].

Figure 9 shows the ratio of current change depending on oxygen. The currents between surface electrodes were increasing as oxygen gas was introduced into chamber. As the concentration of oxygen was kept constant, the sample currents saturated. The currents returned the initial value after oxygen in chamber was exhausted.

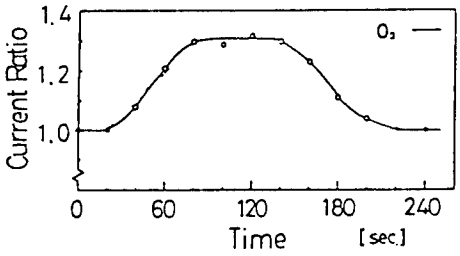

Fig.9 Gas sensitive properties of YSZ film.

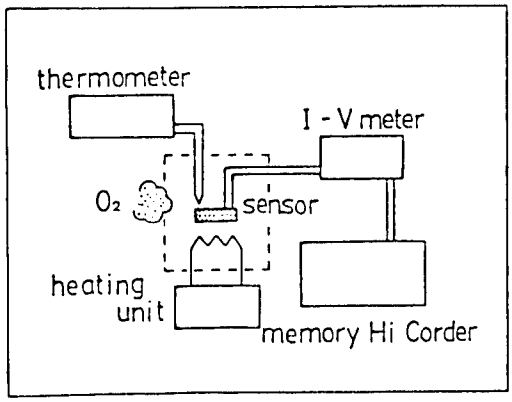

Fig.8 The schematic representation of experimental setup.

CONCLUSIONS

YSZ thin films were obtained by means of R.F. magnetron sputtering using sintered YSZ targets. The film composition ratio corresponded to that of the target. Crystallinity of films depended on the substrate temperature. The phase of film was dominated by the amount of doped Y_2O_3 in the target. The transmission factor was more than 70 % in the range from 300 to 700 [nm], and optical energy gap was ~4.4 [eV]. The resistivity was ~$2.23*10^{-3}$[Ω·cm],and dielectric constant was found to be 24.5~28.6. Using this YSZ film as buffer layer, the superconducting properties of Y-Ba-Cu-O was observed. Surface currents changed depending on oxygen.

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A NEW ARAMID/EPOXY LAMINATE FOR SURFACE MOUNT TECHNOLOGY

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Abstract

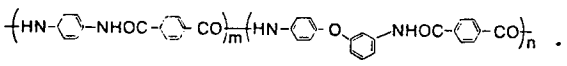
A new aramid/epoxy laminate for use in advanced surface mount technology was developed. The laminate consists of paper from PPDETA (Poly-p-phenylene/3,4'-diphenylether terephthalamide) and epoxy resin with high purity and high temperature resistance. Since the laminate is designed and processed to have minimum impurities, high glass transition temperature, and high dimensional stability, the laminate can be used as a substrate for LCCC, COB, PGA, and other advanced surface mount technologies. Reliability of the laminate to electromigration between surface conductors, between plated-through barrels, and between opposed conductors is one of the highest available today. These behaviors are related to the high purity and high temperature resistance of both the reinforcement material and the resin. The short life of through hole plating in thermal shocks is improved by the application of a new plating technology and a composite structure. Applications to multilayer boards and laminates with a low dielectric constant are also being investigated.

1. Introduction

The need for higher density interconnections of printed wiring boards is increasing, especially in applications for advanced surface mount technologies, such as LCCC, PGA, COB, TAB and Flip Chip.

A new laminate for the advanced surface mount technologies is developed from a newly developed aramid fiber, Technora®, and a newly developed epoxy resin.

Technora®, which will hereafter be referred to as "New Aramid" fiber, is a new kind of aramid fiber with high tenacity and high modulus. It is made from PPDETA, poly-p-phenylene/3,4'-diphenylether terephthalamide,



Since the New Aramid fiber proved to have extraordinarily high adaptability to copper-clad laminates for printed wiring boards, especially in terms of reliability and stability, extensive efforts were made to develop the new laminate, "TL-01," [1, 2, 4], to be used for the advanced surface mount technology. The new epoxy resin formulation was designed to have high affinity to the New Aramid fiber, high temperature resistance, and low ionic impurities. The reliability of "TL-01" to surface electromigration was reported elsewhere [2], and the machinability, the dimensional stability, and the plated-through hole reliability of the laminate were partially reported [3].

In this report, further studies are made to clarify the factors influencing reliability to migration between surface conductors, between plated-through hole barrels and between opposing conductors. Factors influencing the plate-through reliability is also being investigated, and a new structure improving durability to thermal shock is being proposed.

Applications for double-sided boards, multilayer boards, and low dielectric boards are introduced with reference to data obtained in laboratories, as well as in some actual plants.

2. Features of the New Aramid fiber

Specific features of the New Aramid fiber, low impurities, less tendency to fibrillate, and high chemical resistance, originate in a chemical structure of the polymer and the possibility to practice solution spinning. The general performance of the New Aramid fiber from PPDETA is listed in Table 1. The high tenacity, high modulus, and low water absorption are the specific nature of the fiber. Since the fiber has a relatively even microstructure with indistinct crystalline and amorphous regions [5], it is less susceptible to micro-fibrillation that occurs more generally in PPTA fibers.

The impurity levels of the New Aramid fiber is compared to other reinforcements in Table 2, and it is confirmed that the New Aramid fiber has fewer extracted ions than PPTA and glass fibers.

3. Development of "TL-01"

A new laminate, TL-01, was developed by impregnating a paper made of the New Aramid fiber with the newly developed epoxy resin [2]. The

Table 1 Physical properties of Technora® fiber

Color	gold	
Diameter	12	μm
Tensile strength	310	kg/mm^2
Tensile modulus	7100	kg/mm^2
Elongation to break	4.4	%
Thermal decomposing temperature	500	^oC
Heat of combustion	6800	cal/g
Specific heat	0.26	cal/g
Equilibrium moisture content	2.0	%

Table 2 Extracted ions from reinforcements [2]

(μg/g)

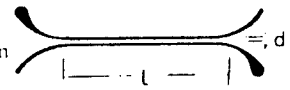
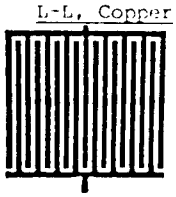
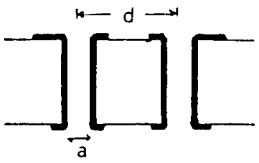
Reinforcement	Na^+	Cl^-
New Aramid fiber	2.0	5.7
PPTA fiber	110	24.1
Glass fabric	36.4	19.1

Table 3 Extracted ions from resins [2]

(μg/g)

Resin	Na^+	Cl^-
New resin	3.5	5.0
FR-4 resin	16.5	200

Table 4 Test conditions of the migration experiments

	Type A L-L, Silver	Type B L-L, Copper	Type C H-H, Copper	Type D S-S, Silver
Configuration				
Dimensions	Spacing, d: 0.5 mm Length, l: 50 mm	Spacing: 0.15 mm Width: 0.3 mm	Diameter, a: 0.4 mm Distance, d: 1.0 mm	Thickness: 0.4 mm
Environment	121 °C, 2 atm.	121 °C, 2 atm.	85 °C, 85 %RH	121 °C, 2 atm.
Bias voltage	90 V	90 V	300 V	90 V

paper base was employed, because it has a better impregnation property, a higher dimensional stability and a smoother outside surface than a fabric base [6]. The resin was carefully formulated in consideration of its affinity to the fiber, temperature resistance, ionic impurities and flammability. In Table 3, the impurity level of the new resin is compared to that of the FR-4 resin. Since the developed resin has a hydrophobic nature, the laminates thereof show excellent electric properties and resistance to soldering.

The features of "TL-01" are as follows:

(1) Excellent reliability to electromigration between surface conductors---even for silver electrodes.

(2) Low X-Y thermal and hygroscopic expansion---CTE as low as 6.5 ppm/°C and CHE as low as 7 ppm/%RH [1].

(3) High temperature resistance---T_g as high as 194 °C [2], and temperature index recognized as 140 °C by UL.

(4) Low dielectric constant---Dielectric constant as low as 3.9 [2].

(5) Low flammability---UL 94V-0 recognized.

Because of these features, TL-01 was first employed in COB mounting technology [3], where high reliability to migration and corrosion is imperative. The machinability of the laminate was confirmed to be almost equivalent to FR-4 in terms of drilling, plating, routing, and shearing performances, if the processing conditions are properly selected. However, some questions were left in promoting applications, especially in reliability to other types of electromigration, plated-through hole reliability, and processability of multilayer boards.

4. Factors Influencing Reliability to Electromigration in Some Configurations

Electromigration behavior of laminates was investigated for four kinds of reinforcements combined with two kinds of resins. For reinforcement material, fabric and paper made of the New Aramid fiber were used together with glass fabric and PPTA fabric. For resin, the newly-developed epoxy resin with high purity and high temperature resistance was used together with the conventional resin employed in FR-4, which will be hereafter referred to as "FR-4 resin."

The electromigration of copper and silver electrodes was investigated for three kinds of configurations [7]:

(1) Line-to-Line (L-L), between surface conductors on the same side of the circuit.

(2) Hole-to-Hole (H-H), between plated-through hole barrels.

(3) Surface-to-surface (S-S), between surface conductors on opposite sides of the circuit.

The test conditions of electromigration are

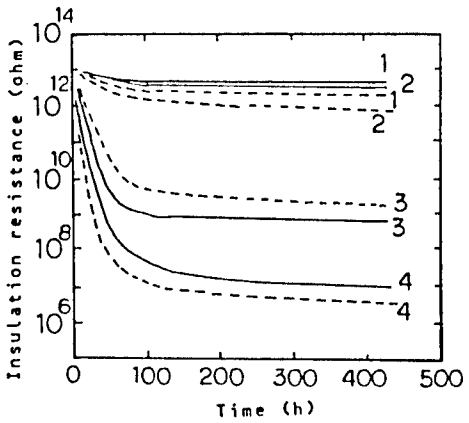


Figure 1 Insulation resistance of laminates between silver electrodes (Type A migration)
1: New Aramid paper, 2: New Aramid fabric, 3: Glass fabric, 4: PPTA fabric, ——: New resin, ----: FR-4 resin.

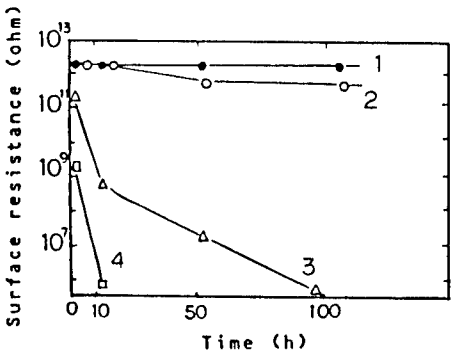


Figure 2 Insulation resistance of laminates between copper electrodes (Type B migration)
Codes same as Figure 1.

listed in Table 4. For the L-L configuration, silver and copper electrodes were employed, and for the S-S configuration, silver electrodes were employed, since silver is more susceptible to electromigration than copper [8]. It is usually used for die bonding of semiconductor chips in direct mount technology.

In Figure 1, the insulation resistance between silver electrodes (L-L configuration) is plotted against time, and in Figure 2, results for the copper electrodes (L-L configuration) are shown. In these tests, solder resist was not applied. Results for the H-H configuration are sown in Figures 3.

In the L-L and S-S configurations, the migration phenomena is drastically influenced by the reinforcement material [2], while in the H-H configuration, the migration is influenced mainly by the resin. It is to be noted that the fabric

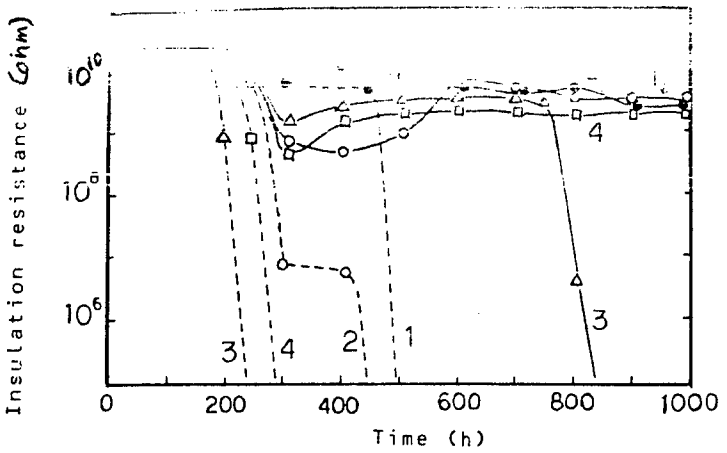


Figure 3 Insulation resistance between plated through-holes (Type C migration) Codes same as Figure 1.

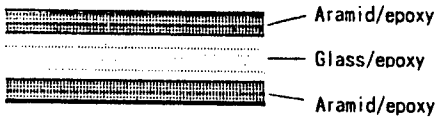


Figure 4 Composite laminate

base is more susceptible to electromigration than the paper base. Considering that the fiber length is a few millimeters and the hole-to-hole distance of the H-H configuration is only 1 mm, this difference is ascribable to the better impregnation property of paper than fabric. In all configurations, it was confirmed that the combination of the New Aramid and the new resin, which stands for TL-01, is the least susceptible to electromigration, and in all test conditions employed here, no migration was ever observed in this combination.

Looking closely at this migration phenomena, it is concluded that the interface affinity of fiber and resin plays an important role. In the case of a glass-base laminate, the interface is susceptible to migration, and in the initial stage, the fiber is coated with black silver oxide or copper oxide, and over-all migration or shortage occurs afterwards. The results in Figure 3 suggests some contribution of pore structures, since fabrics, which has very small intra-yarn pores, usually have poorer impregnation property than papers.

5. Aramid/Glass Composite---A Realistic Solution

It has been pointed out that aramid-base laminates have higher Z-direction expansion due to higher CTE of the aramid fiber in the direction perpendicular to the fiber axis [9], and less durability of through hole plating to thermal shocks than the FR-4 or the glass/polyimide laminates. Although it may be impossible to decrease the perpendicular CTE of the aramid fiber, some new technologies were applied to improve the durability of the plating.

New plating technologies developed for higher aspect ratio through holes were applied to TL-01, and it was found out that some of them were useful in improving the durability as shown in Figure 5.

The other solution is a composite structure with glass/epoxy layers inside as shown in Figure 4. This structure can be applied for double-sided copper clad laminate, when the laminate is used for the applications where low thermal expansion of the laminate is not imperative. The experimental results in the last chapter indicate that the H-H migration can be alleviated by using the new resin, which has low ionic impurities and high temperature resistance. The aramid/epoxy layer on both tops of the laminate will make the laminate less susceptible to surface migration and also make the surface smoother. In case the semiconductor chips are mounted directly on the board, the top layer

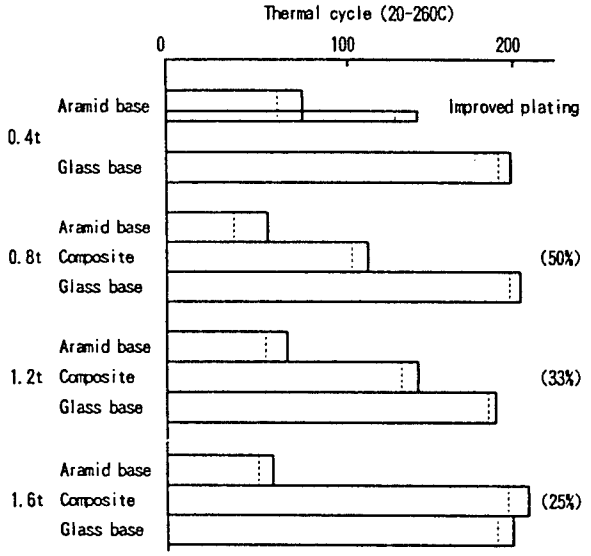


Figure 5 Durability of plated-through holes to thermal shock. Figures in the parentheses are volume fraction of aramid-base layers.

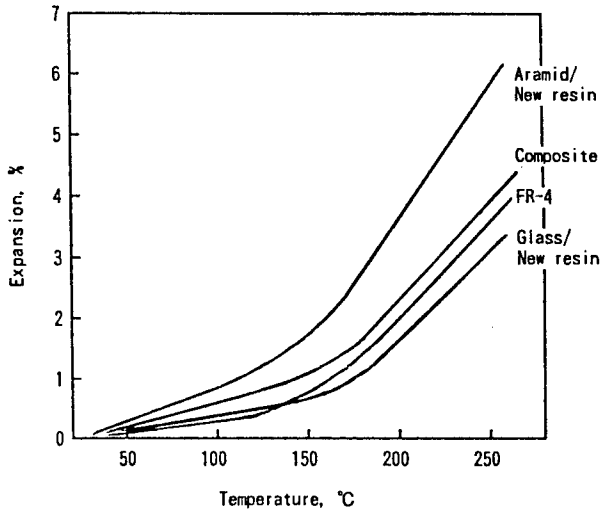


Figure 6 Z-direction expansion of aramid-base, glass-base and composite laminates

will prevent corrosion of semiconductor chips due to ionic contamination emanating from the glass

[illegible]. The stress of die bonding due to the difference of CTE values will be smaller than FR-4 to some extent.

The test results of the through hole reliability to thermal shock is shown in Figure 5. It is clear that the durability of the composite structure is better than the aramid/epoxy laminate, and the life increases as the volume fraction of the aramid layers decreases. In Figure 6, the expansion of the aramid, glass and the composite laminates is plotted against temperature. It is shown that the expansion of the composite laminate is almost same as FR-4 at high temperatures, presumably because of the lower CTE value and the higher glass transition temperature of the resin.

6. Multilayers---Better Processability

For higher end-uses, the fabrication of multilayers from TL-01 and prepregs is necessary. The processability of TL-01 for multilayers was tested in labs and actual fabrication plants. Double-sided copper clad laminates, having a length of 50 cm on each side, were etched, treated by black oxides, and dried at high temperatures. The etched laminates were piled up together with copper foils on both tops and prepregs and press-cured to form a six-layer board.

The registration was measured using a two-dimensional coordinate measuring instrument. Comparison to FR-4 revealed that the dimensional stability of TL-01 was much higher than FR-4, as shown in Figure 7.

After the lamination was over, the board was inspected by taking soft X-ray pictures at the center and the four corners. As shown in Figure 8, there was no remarkable aberration of circuits on these layers.

7. Low Dielectric Board---Future Development

A lower dielectric constant is required in laminates for higher speed transmission. In Figure 9, dielectric constant and dissipation factor of the laminates with a New Aramid base are compared to those with a glass base. The laminates with the New Aramid base have a lower dielectric constant than those with the glass base, and it is expected that the New Aramid is used for high-speed transmission by impregnating low dielectric resins, such as polycyanurates.

8. Conclusions

The base construction for the development of laminates from the New Aramid is completed, and the material innovation in interconnections and printed wiring boards has just made a start.

Diversification of the aramid-based laminates will be needed in the near future, in response to increasing end-uses. These include metal-base laminates, semi-flexible multilayers, rigid-flex laminates, and thermal conductive laminates.

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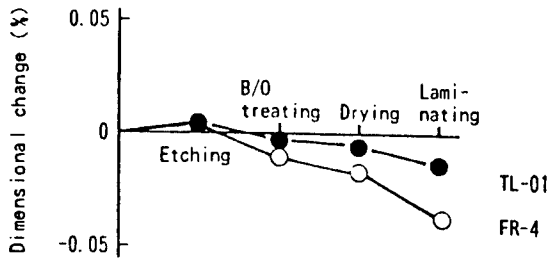

Figure 7 Dimensional stability of aramid-base(●) and FR-4 (○)laminates

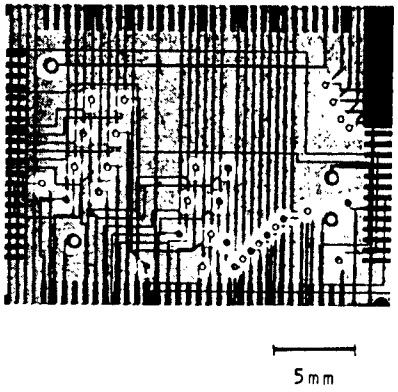

Figure 8 X-ray photograph of aramid-base multilayer board

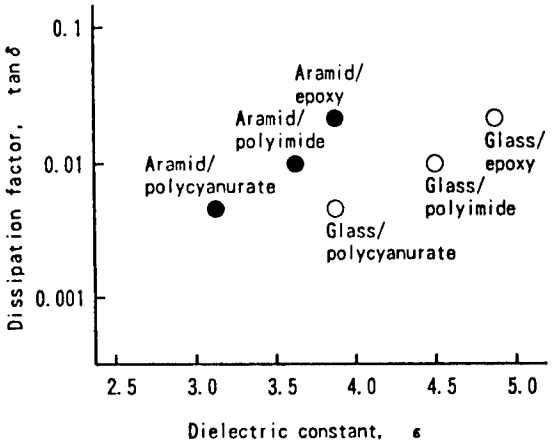

Figure 9 Dielectric constant and dissipation factor of aramid-base and glass-base laminates

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Applications of New Assembly Method "Micron Bump Bonding Method"

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ABSTRACT

A new LSI chip bonding method named " Micron-Bump Bonding Method " was developed. and by this, the micron order direct bonding between the LSI electrode and the electrode provided on the circuit substrate became feasible.

The shrinkage stress generated in light setting insulating resin is utilized. to apply a compressive force on a LSI chip against the electrodes provided on a substrate in this method. LSI chips having an inter-electrode spacing of 10 microns and 2320 electrodes in total was successfully gang bonded in a face-down from with high reliabilities. And, this technology was successfuly applied to the LED array head.

INTRODUCTION

As typically seen in recent driver LSI developed for display, tendency of the increased number of LSI electrode pins while its decreased pitch, yet the increased chip size are evident. These are inevitable to make the electronic apparatus thinner, lighter, and more compact, and thus, it is essential to develop new technologies to assemble LSI of super-multi-pins of narrow pitch. Whereas the conventional assembling method includes the wire bonding, TAB. and the flip-chip methods which had been developed and practiced for years, the smallest pitch presently practical is approximately 80 microns even by the TAB method. As for a solution for this problem. we developed a Micron-Bump Bonding method by which 10 micron pitch LSI electrodes and the electrodes provided on the circuit substrate can be connected by means of a light-setting resin, and reported previously [1].

In the course of expanding the application field of this Micron-Bump Bonding method. we recently experimented the bonding of optical devices, or LED array module employed for LED printer head by this method.

The light emitting diodes are arranged in a row at the density of 400 DPI (63.5 micron pitch), and 54 each LED array chips and corresponding 54 driver IC chips are arranged for one LED printer head on a 246mm×14mm glass substrate, and thereby the bonding have to be performed at 12,944 points.

This paper reports on the results of an experiment conducted to confirm the applicability of Micron-Bump Bonding method for LED array assembling where 54 chips disposed at a close inter chip distance of 10 microns have to be bonded, and also confirm the effects of bonding on its light emissivity and heat dissipation.

OUTLINE OF MICRON-BUMP BONDING METHOD

Structure and Principle

Structure

Fig. 1 shows a cross-section of chip and substrate bonded by this bonding method where a LSI having gold bumps is adhered on a circuit substrate by means of a light setting insulating resin. The gold bumps and the circuit formed on the substrate are pressed each other to establish an electrical connection by the contracting stress produced in the light-setting insulating resin.

Principle

Fig. 2 illustrates the principle of bonding acted by Micron-Bump Bonding method where the following relation has to be established.

$$\alpha, \beta \rangle W \rangle P$$

where;

- α : Adhesive stress acting between the resin and LSI chip.
- β : Adhesive stress acting between the resin and circuit substrate.
- W : Contracting stress of resin

P : Thermal stress of resin

The above relationship can be maintained by controlling the physical characteristics of the employed light-setting insulating resin.

Features

Followings are the advantages achieved by the Micron-Bump Bonding.

1) Gang bonding of micron order pitch can be achieved.
   Gang bonding of 2320 electrodes of 10 micron pitch was experimentally confirmed.
2) High reliability
   Since the bonded point consisted of gold bump and substrate electrode is not permanently fixed,the thermal stress induced by differential thermal expansion is absorbed therein.
3) Replacement of LSI is possible.
4) No thermal energy is required for the bonding.
5) Simple process and thus resulting in low cost.

Bonding Process Flow

Fig. 3 shows a flow-chart of Micron-Bump Bonding process. The process is started with the coating of substrate by a light-setting resin, and this is followed by the alignment of a LSI chip electrodes and the substrate electrodes. The LSI chip is then pressed against the substrate to squeeze the resin under the bumps to establish an electrical connection between bumps and

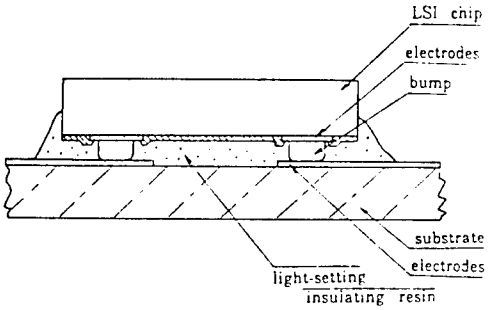


Fig.1 Cross-sectional of bonded LSI chip by this new method.

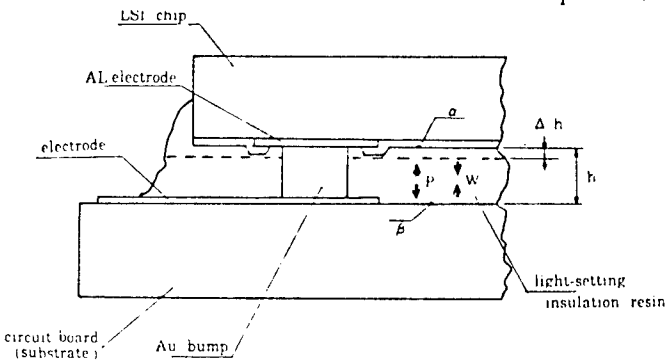


Fig. 2 Principle of New Method

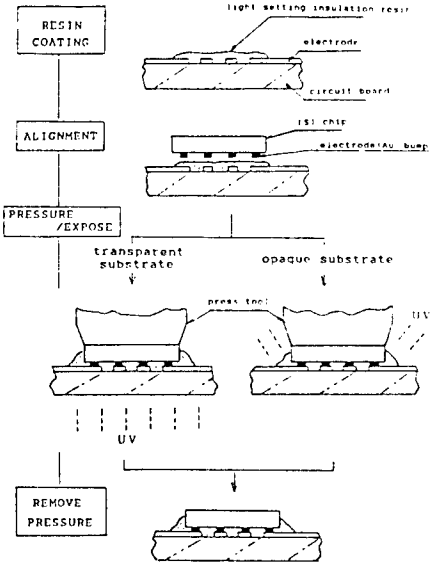
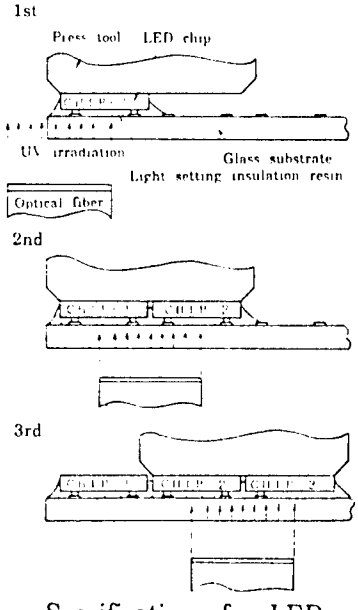


Fig.3 Process flow of "Micron-Bump Bonding Method"

	LED	IC
Size	4.06×0.5 mm²	1.69×4.31 mm²
Pitch	635 μm	100 μm
Pin count	126	110
Dot count	64	—

Fig.5 Process flow for narrow chip-gap bonding



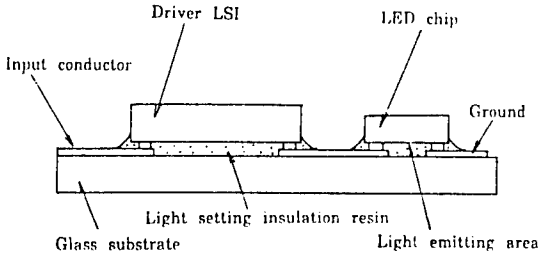


Fig.4 Cross-sectional of LED array module by "Micron-Bump Bonding Method".

Table.1 Specifications for LED array and driver LSI.

substrate electrodes.

The resin in the transparent substrate region is set by UV irradiation while the LSI is pressed at a stationary condition, and the resin in the rest of substrate region is set at room temperature.

LED ARRAY MODULE

Since the LED printer is one of the optical printers featuring its compact structure and high printing speed, it should be very popular in near future. However, the LED array module used in LED printer has been assembled by a conventional wire-bonding method which required chip electrodes to be disposed at a zigzag pattern while the light-emitting diodes are disposed linearly at 63.5 micron pitch, and this inevitably required to provide a large chip area for wire bonding.

Since the electrode bump can be disposed on a line making a 1 : 1 correspondence to the light emitting diodes, the LED array module developed for the Micron-Bump Bonding features; 1) smaller chip area thus the lower cost, 2) possibility of still higher density, and 3) compact size.

Constitution of LED Array

Fig. 4. shows a cross-sectional structure of LED array module assembled by Micron-Bonding Bondding method. The 64 dots LED array chip the driver IC both having gold bumps are mounted at 1 : 1 relationship on a glass substrate. Therefore, for constructing A-size LED, 54 each LED array and driver ICs are required to be bonded.

With the structure above shown, the light emitted from LED passes through both light-setting resin and glass substrate before going into a Selfoc lens mounted externally. As external circuit and heat radiator have to be further added to form a LED printer head.

Material Considerations

Light-setting insulating resin

The employed light-setting resin consists of a denatured acrylate resin developed by considering the bondability and light transmittance which is 100% for the LED emitting light having a wavelength of 660nm. And an aging effect of the light emissivity indicating no degradation after 125°c, 1000hour exposure.

LSI chip and bump

Table 1 shows the specifications for the LED array and the driver IC chips. the gold bumps are formed by electroplating in their wafer process.

Circuit substrate

SiO_2 is deposited on the sodium-glass circuit substrate in order to eliminate the effect of sodium contained therein, and the wiring is prepared by 2.5 micron thick gold thick-film considering the specific resistance and the cost. The size of the substrate is 236mm×14mm, with a thickness of 1.1mm.

Consideration on process Conditions

Condition for narrow chip-gap bonding

The dot pitch is 63.5 microns for 400 DPI LED printer head, thus, this dot pitch has to be realized even between each dot nesting on the edge of neighboring chip, and this means that the chip must be placed at the minimum permissible distance of approximately 10 microns.

Fig. 5 shows the flow-chart for this narrow chip-gap bonding where the chip pressing is performed for one each chip and the UV irradiation is conducted for only a half portion of the pressed chip so that the effects of excess resin oozed out sideways toward the neighboring chip can be minimized.

Evaluation of Electrical Characteristics

The electrical characteristics of modules assembled under the above described condition are evaluated, and are described below.

V-I characteristics of LED

The V-I characteristics of LED before and after the bonding are shown in Fig. 6 which shows virtually no difference, and thus, no effects on the contact resistance is affected by the pressing.

Light-emitting characteristics

Fig. 7 is measured emitting light distribution showing very little light spreading, and this shows also very little light scattering during the light transmission through the light-setting resin and glass substrate.

Heat dissipation

The degree of temperature rise when all 54 LEDs mounted together with 54 driver ICs on a A-size LED array head are energized and a current of 3 mA is fed through each of 3456 bonding dots at a same time is measured, and found it was less that 40°c which is considered

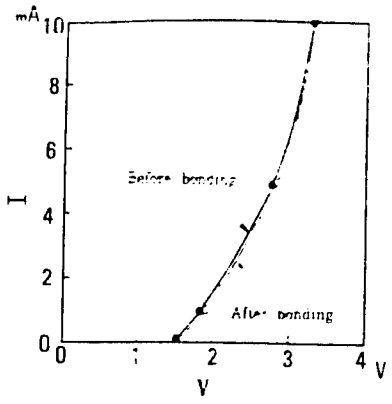


Fig.6 V-I characteristics of LED

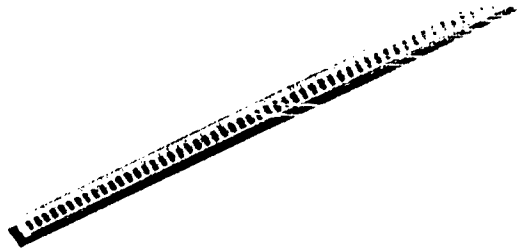


Photo.1 LED array module.

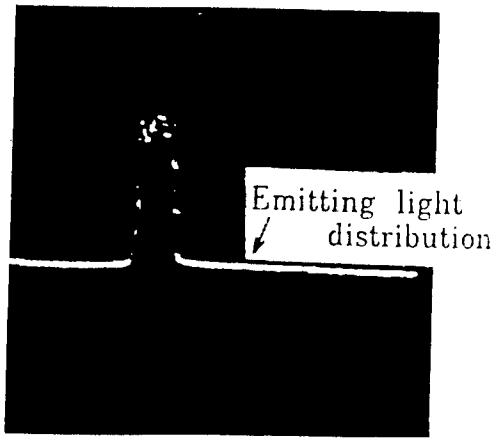


Fig.7 Light-emitting characteristics satisfactory.

N = 240chips

Test items	Condition	Failures
High temprature strage	125°C 1000H	0/240
High temprature / High Humidity strage	85°C 85% 1000H	0/240
Thermal shock	-55°C 125°C 100cycles	0/240

Table.2 Results of reliability tests

Fabrication Tests

Experimental fabrication of A-size LED array modules shown in photo 1 was conducted under the above described process condition, and bonding yield of 99.8% was obtained after approximately 2000 LSI chips were bonded. Analysis then found that the environmental dusts were entirely responsible for these bonding failures, and then it is essential to perform such a fine bonding work in the environment of improved cleanliness.

Reliability evaluation

The results of bonding reliability tests and the aging effects of light emission characteristics were found satisfactory as shown in Table 2.

CONCLUSION

In order to study the applicability of Micron-Bump Bonding method on the optical devices, the material and process to constitute the LED array module and its electrical characteristics and heat dissipation were experimented and evaluated, and was found practically applicable.

Future experiments for the the high speed device, power device and larger chip-area device are scheduled for extending its application fields.

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A NEW PACKAGING CONCEPT FOR HIGH DENSITY MEMORY MODULES

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[ABSTRACT]

High density memory modules have been fabricated utilizing a new LSI interconnection method. In this module, a new LSI chip was conceived whose bonding pads are formed on the device active area. This LSI chip was accomplished by an on-device multilayer wiring process, consisting of forming a polyimide insulating layer and thin metal film conductor layers (Ti/Ni/Au) which have new pads for connection.

A feasibility study has been carried out on this LSI chip. Defect analysis was carried out for the polyimide insulating layer and the conductor layers to establish the process for this LSI chip. The influence of each process upon the device characteristics was evaluated with AC/DC parameters and T.E.G. parameters at 4 steps in the whole process. Five kinds of reliability tests, high temperature storage test, high temperature high humidity test, temperature cycle test, high temperature operation test, and high temperature bias test, were carried out. This LSI chip sucessfully satisfied the specifications and passed the reliability tests.

[INTRODUCTION]

The distribution of LSI chips and wirings is not so flexible conventionally in the chip-on-board (COB) technology, since the design for interconnecting wirings among LSI chips depends on the pad layout. Also, when the area for distributing wirings is enlarged with an increase in the number of interconnecting wirings, this enlarged area interferes with the LSI chip mounting density. These two factors, poor flexibility and interference with the density, hinder improving the semiconductor packaging density.

Recently, the authors have come to a satisfactory settlement of these problems and have developed a new packaging concept. We have also fabricated a high density memory module utilizing the printed wiring connection (PWC) method.[1] In this module, five 256 kb SRAM chips are embedded flush and close together in the module substrate. Conductive polymer paste wirings interconnecting LSI chips are formed on the chips by screen printing.

A high density memory module can be easily accomplished in this concept, since interconnecting wirings occupy only a confined area which is equal to the total chip area. Post-processing was found to be required to form wirings upon the LSI chips in order realize this high density module. In this new post-process, bonding pads were rearranged on the device active area so that the pad layout would be suitable for high density packaging. These pad rearrangments were accomplished by an on-device multilayer wiring process, consisting of forming a polyimide insulating layer and thin metal conductor layers (Ti/Ni/Au) which have new pads for connection. The size of these rearranged pads was expanded nine times larger than the original pad to facilitate screen mask alignment in the PWC method.

This paper describes the process for pad formation upon the active area of the LSI chip, indicates the characterictics and reliability of the post-processed chips, and refers to the degree of assembling area shrinkage compared with conventional COB technology.

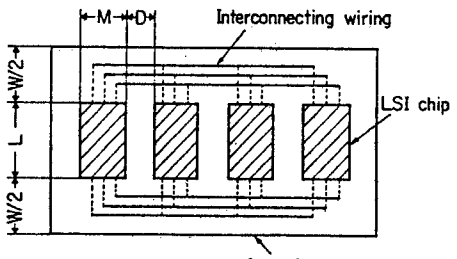
[BACKGROUND]

Interconnecting wirings among LSI chips are conventionally formed between the LSI bonding pads and secondary bonding pads on the printed circuit board. Because these wirings are formed around the chips, it is necessary to use a large area to interconnect among LSI chips.

Figure 1 shows the area for the chips and their interconnecting wirings in the method using conventional COB technology. As shown in this figure, LSI chips are mounted so that they are separate from each other with a space D, and interconnecting wirings are formed around the chips with width W. The total interconnecting wirings area for packaging is several times larger than the area for the chips described by the following equation.

$$r = \frac{Sw}{Sc} = \frac{n\{WM+D(W+L)\}}{nLM}$$

L,M : chip size



Ratio of interconnecting wiring area to chip area

$$\gamma = \frac{Sw}{Sc} = \frac{n\{WM+D(W+L)\}}{nLM}$$

L,M: chip size
D : chip space
W : wiring width
n : number of chips
Sw: area for interconnecting wirings
Sc : chip area

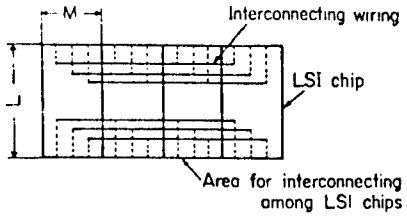
FIG. 1 Area for interconnecting among LSI chips, in the method using COB technology

D : chip space
W : wiring width
n : number of chips
Sw : area for interconnecting wirings
Sc : chip area
r : ratio of interconnecting wiring area to chip area

The interconnecting wiring area will increase in proportion to the wiring width (depending on the number of wirings) and to the number of mounted chips. This extra but indispensable area for interconnecting among LSI chips interferes with the device mounting density when the number of mounted chips are increased.

Recently, the authors have developed a high density memory module employing a new concept, as shown in Fig.2. In this concept, LSI chips are mounted flush and close together on the module substrate, and interconnecting wirings among the LSI chips are formed in plural parallel lines on the active area of the chips. In this method, the area for packaging can shrink as far as the total area for the chips, since the interconnecting wirings among the LSI chips are formed on the device active area. A new LSI chip with rearranged pads, as shown in Fig.3, was required to form the interconnecting wirings on the device active area. In this new device, these rearranged pads are nine times larger than the original pads on the device active area to facilitate the alignment, and the pad layout is suitable for on-device wiring formation. However, when interconnect wirings among the LSI chips are formed on a device active area, it is important to consider the effect of any damage to the devices under the rearranged bonding pads. The device characteristics will be changed if a high power and high temperature technique, such as wire-bonding or the TAB method was used to interconnect these chips. The previous report indicated that, using this PWC method, LSI chips would be connected with each other without damage, because the interconnecting wirings among LSI chips are formed at low temperature and with no force. Further more, this method is expected to have the following advantages,
(1) A smooth-surface can be easily fabricated, since interconnection is formed by flat wirings.
(2) It is possible to reduce packaging cost ,since interconnections are formed similtaneously ,irrespective of the number of LSI chip bonding pads.
(3) The packaging cost is much lower than that for conventional packages, which are made by TAB or the wire-bonding method.

Figure 4 shows a top view of a high density memory module and its new LSI chips that are fabricated with this new packaging concept.



Ratio of interconnecting wiring area to chip area

$$\gamma = \frac{Sw}{Sc} = \frac{nLM}{nLM} = 1$$

L,M : chip size
n : number of chips
Sw : area for interconnecting wirings
Sc : chip area

FIG. 2 Area for interconnecting among LSI chips, in the method using new concept

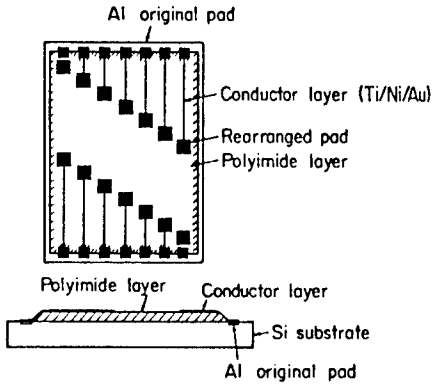


FIG. 3 Top and cross sectional views of LSI chips

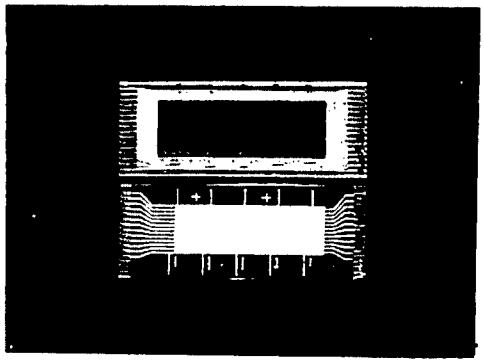


FIG.4 Top view of high density memory module

[EXPERIMENTAL]

[1] Rearranged pad formation

The post-process for the new pad formation is, in general, realized by the following four process steps. The first step is the formation of a polyimide insulating layer. Second is a pretreatment before deposition for the conductor layer. The third step is conductor layer formation including the rearranged pad. The final step is annealing process. The process sequence is shown in Fig.5.

[1-1] Polyimide insulating film formation

First of all, a photosensitive polyimide precursor, "Toray Photoneece 3140", was spin coated onto a prepared 256 kb SRAM wafer at 3000 rpm for 30 seconds at 25 ℃, and was prebaked at 80 ℃ for 30 minutes. Then, "Toray Photoneece 3140" was exposed, using a contact exposure system. The development process and the rinse process was accomplished by batch immersion ultrasonic application. The developer was "Photoneece developer DV-505" and the rinser was isopropylalcohol. The postbake was accomplished by baking for 30 minutes at 150 ℃, 30 minutes at 250 ℃ and for 30 minutes at 400 ℃ in nitrogen. The polyimide insulating layer was thus formed.

[1-2] Pretreatment before deposition

Plasma etching was accomplished before the the deposition process for a conductor layer to remove any poyimide residue remaining on the Al bonding pads. A slight Al etching was

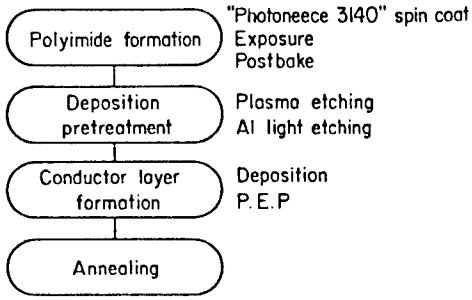


FIG. 5 Process sequence for pad formation

carried out to remove the Al oxide film on the Al bonding pads which was formed when the wafer was burned at high temperature. Here, the Al bonding pad is composed of an Al alloy, Al-1%Si-0.5%Cu.

[1-3] Conductor layer formation

The conductor layer including the rearranged pads was composed of Ti(1000A)/Ni(3000A)/Au(5000A). Here, the Ti layer was used as adhesive material, the Ni layer was the barrier metal between the Al layer and the Au layer, and the Au layer was used as contact metal with the polymeric paste. These layers were deposited by the E-gun evaporation method with EVC 700B (ANELVA). Then, the layers were patterned with the etchant shown in Table 1. In the final process, the devices were annealed at 380 ℃ for 30 minutes in nitrogen atmosphere.

TABLE 1 Etchant for Ti/Ni/Au

Material	Etchant		Temperature
Au	KI	40g	20°C
	I_2	10g	
	H_2O	40ml	
Ni	CH_3OH	750ml	20°C
	HCl	750ml	
	$CuSO_4$	150g	
	H_2O	750ml	
Ti	NH_3	70ml	60°C
	H_2O_2	100ml	
	EDTA	92g	
	H_2O	400ml	

[2] Interfacial analysis

The interface Al/Ti/Ni/Au layers were analyzed by Auger electron spectroscopy (AES), thin film X-ray diffraction (XRD), X ray photspectroscopy (XPS), and an electron probe microanalyzer (EPMA). Diffusion profiles were analyzed with the Ar ion sputter etching technique in AES, and the thin surface layer crystal structure was analyzed with the low angle X-ray irradiation technique in XRD. The identification of polyimide residue on the Al bonding pad surface was analyzed by XPS, and the factors corroding Al bonding pads were analyzed with EPMA.

[3] Device characteristic evaluations

AC/DC parameters and T.E.G. parameters were measured to evaluate the influence of each process upon the device characteristics. The whole process was composed of 4 steps. First a polyimide insulating film was formed. Next, plasma etching was carried out, a conductor layer was formed and finally an annealing process was carried out. These parameters were measured as shown in Table 2.

Be-Cu probe pins were used, when probing the rearranged pads, to avoid damage to the devices under the rearranged pad. A memory tester T3331B-T5 (ADVANTEST) was used for the AC/DC parameter measurement at 0.5 V interval step loops, using the Row Fast Scan March as a test pattern at room temperature. T.E.G. parameters were measured with a semiconductor parameter analyzer (YHP).

TABLE 2 Measurement items for device characteristics

T.E.G. parameters		AC/DC parameters	
Characteristics	Symbols	Characteristics	Symbols
V_{TH} N 4/1.2	N_{ch} V_{th}	Standby current	IDDS
V_{TH} P 4.2/1.2	P_{ch} V_{th}	Operating current	IDDO
V_{PT} N 100/1.5	N_{ch} V_{PT}	Address access time	tACC
I_{DO} N 4/1.2(NOR)	$N_{ch}I_{DO}$ (NOR)	$\overline{OE}$ access time	tOE
I_{DO} N 4/1.2(REV)	$N_{ch}I_{DO}$ (REV)	$\overline{CE}$ access time	tCO
I_{DO} P 4.2/1.2	P_{ch} I_{DO}	Power supply voltage Max. Min.	V_{DD} Max. V_{DD} Min.

[4] Reliability test

Five kinds of reliability tests, high temperature storage test, high temperature high humidity test, temperature cycle test, high temperature operation test, and high temperature bias test were carried out under the condition shown in Table 3. Differences in the tested AC/DC parameters and T.E.G. parameters from their initial values were measured. The number of defectives were measured from the difference between the initial value and the final value in the reliability test. The criteria for defects were defined as indicated in Table 4 to decide the acceptability of the device.

TABLE 3 Reliability test items and conditions

Type	Test items	Content and condition of test
Life time test	High temperature operation test	Apply electrical stress and thermal stress to elements for extended period. Device durability determinded for T_a=125°C,V_{DD}=6.0V
	High temperature storage test	Ability to withstand heat when stored under high temperature for extended period determined for T_a=150°C
	High temperature high humidity storage test	Ability to withstand high temperature and high humidity for extended period T_a=85°C, RH=85%
	High temperature bias test	Apply electrical stress and thermal stress to elements for extended period. Device durability determined for T_a=125°C,V_{DD}=6.0V
Environmental test	Temperature cycle test	Ability to withstand cyclic low temperature and high temperature determinded for ~55°C ~25°C ~150°C ~25°C (30 min) (5 min) (30 min) (5 min) ← one cycle →

[RESULTS AND DISCUSSIONS]

[1] Polyimide insulating layer

Table 5 shows the characteristics for the polyimide insulating film used in this study. Impurities contained in the films which affect the device characteristics were less than ppm order. Especially uranium was less than ppb order. As the impurities were of an extremely small amount, this polyimide was considered satisfactory for use in semiconductor devices.

Although a polyimide insulating film on phosphorus silicate glass (PSG) was formed, except for Al bonding pads, some polyimide residue usually remained on the Al bonding pad surface, because a photosensitive polyimide precursor reacts with aluminum. An abnormal resistance exsists between the Al bonding pad surface and the conductor metals when the polyimide residue remains on the Al bonding pad surface. Therefore, it is important to remove the polyimide residue from the Al bonding pad surface. Figure 6 shows an analysis by XPS to confirm the plasma etching effect in removing the polyimide residue from the Al bonding pad surface when the polyimide insulating film was formed. Polyimide has an N1s peak at 400 eV which indicates an imide structure. The identification of polyimide can be judged from whether or not this peculiar peak exist. Spectrum #1 shows

TABLE 4 Failure criteria specification for SRAM devices

Symbol	Measurement conditions (T_a=25°C)	Criteria	
		Minimum	Maximum
IDDS	CE=V_{DD}-0.2V, V_{DD}=3.5V~6V	—	50μA
IDDO	V_{DD}=5.5V, CE=0.2V Mini. cycle	—	45mA
tACC	V_{DD}=5V±10%, Marching pattern	—	120nS
tOE	V_{DD}=5V±10%, Marching pattern	—	70nS
tCO	V_{DD}=5V±10%, Marching pattern	—	120nS
V_{DD}	Marching pattern	4.5V	5.5V

the Al bonding pad surface before the polyimide film was formed. The polyimide surface was shown as spectrum #4 for reference. Spectrum #2 shows the analysis result for the Al surface when its surface was not etched by plasma. In this spectrum, it is clear that the polyimide residue remained on the Al bonding pad surface, as the N1s peak appeared at 400 eV resulting in an imide structure. Spectrum #3 shows the result after plasma etching. The polyimide residue was removed, since the N1s peak disappeared. These spectra show that the plasma etching process is an effective method to remove polyimide residues.

Figure 7 shows the relation between the polyimide residue quantity on the Al bonding pad and contact resistance which arose between the Al bonding pad and conductor metal layer. Here, polyimide residue quantity was defined from the N1s peak intensity in XPS normalized by the Al2p peak intensity. And the contact resistance was measured by the 4 point probe method to neglect the resistance in the measurement system. It is obvious from this figure that increasing the N1s peak intensity increase the contact resistance value.

These two facts show that there is some polyimide residue on the Al bonding pad immediately after polyimide films are formed causing abnormal resistance between the Al bonding pads and the contact layers. Also, if plasma etching was carried out, this residue would be removed and the contact resistance would decrease to a range sufficient to satisfy the operating characteristics.

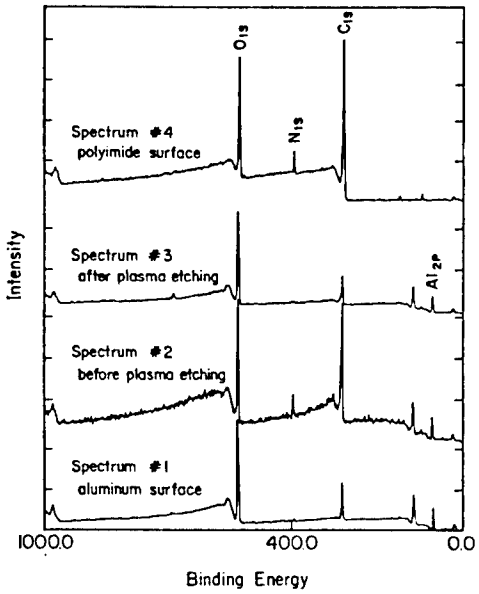


FIG.6 XPS profile on Al bonding pad surface

[2] Ti/Ni/Au conductor layer

Figure 8 shows the depth profile for some elements at the Al/Ti/Ni/Au interface determined by AES. As shown in Fig 8, Al/Ti, Ti/Ni, and Ni/Au diffuse with each other a little, but the Al and Au layers were clearly separated within the AES detective range. If Al-Au diffused with each other, intermetallic compounds, well-known to increase the contact resistance, will be formed due to annealing.[2],[3]. Figure 9 shows X-ray diffraction patterns by XRD to confirm that no intermetallic compounds were formed. Patterns indicated in this figure show that, an intermetallic compound AlAu was formed, this intermetallic compound does not cause an abnormal increase in resistance. And contact resistance value was sufficient to form a conductor layer. On the other hand, if Cr/Au was used for the conductor layers intermetallic compounds which caused abnormal increase in resistance was formed because Au diffused through the Cr layer to the Al layer. These facts show that, if Ti/Ni/Au was used for the conductor layer composition, there would be no problem, because Ni sets up a sufficient barrier to avoid Al-Au intermetallic compounds.

[3] A standard design for pad formation

Al bonding pad corrosion often occurred when the conductive metal layer were patterned. This corrosion caused contact failure between the surface of an Al bonding pad and conductor layers. It is important to clarify how corrosion occurs to obtain high process yields. Table 6 shows the X-ray intensity values analyzed by EPMA for all the elements detected in this area, normalized by phosphorus which was doped in PSG. Comparing the X-ray intensities of Al, Si, and Cu, composing the Al bonding pads, for the corrosion area and the reference area, the X-ray intensity in the corrosion area was smaller than in the

TABLE 5 Polyimide film characteristics

Impurity content	Element	Unit	Measurement value
	Na	ppm	0.05
	K	"	0.07
	Cl	"	0.4
	U	ppb	less than 0.01
Thermal property	**Item**	**Unit**	**Measurement value**
	Coefficient of thermal expansion	1/°C	4×10^{-5}
Electrical property	**Item**	**Unit**	**Measurement value**
	Dielectric constant (1 kHz, 25°C)	—	3.2
	Volume resistivity	Ω·cm	1.3×10^{16}
	Surface resistivity	Ω	10^{16}

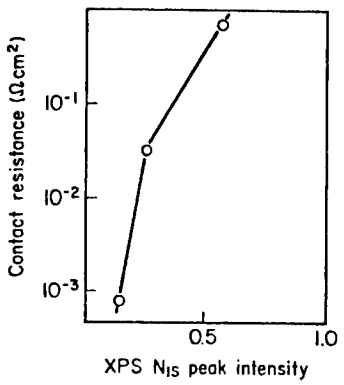


FIG.7 Relationship between contact resistance and polyimide residual quantity on Al bonding pad surface

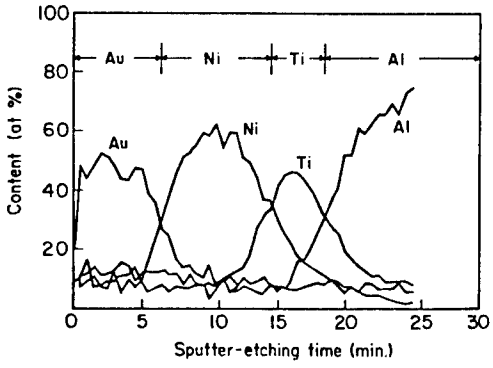


FIG.8 Element profile by Auger electron spectrometer at Al/Ti/Ni/Au interface

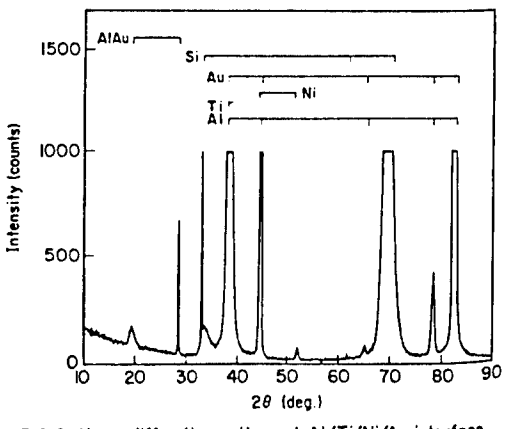


FIG.9 X-ray diffraction pattern at Al/Ti/Ni/Au interface

reference area. This fact supports the fact that contact failure is caused by Al bonding pad corrosion. And the factor that corrodes Al was the Ti etchant, because the element detected from this area did not include iodine or copper, which are components in the Au and Ni etchant.

The mechanism for Al bonding pad corrosion is considered as follows. As described in Fig.10, if Ti was over-etched near the Al bonding pad, when the conductor layer were patterned, the Al bonding pad would be corroded by the Ti etchant intruding into it. This consideration is based on the fact that Ti has a tendency to be over-etched by the etchant.

TABLE 6 X-ray intensity normalized by P doped in PSG

Element & line	Intensity
Refference area	
Al Kα	29.86
Si Kα	20.19
P Kα	1.00
Cu Kα	0.50
Corrosion area	
Al Kα	7.40
Si Kα	12.52
P Kα	1.00
Cu Kα	0.46

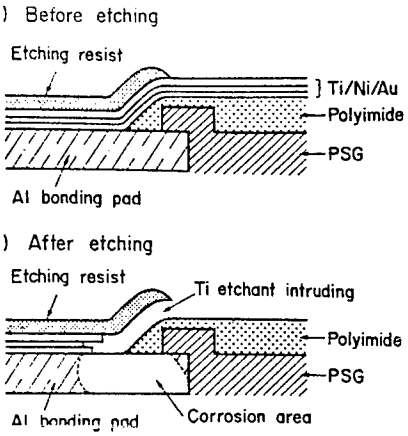
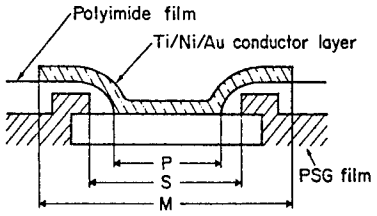


FIG.10 Al bonding pad corrosion mechanism

Figure 11 shows the relation between the corrosion occurrence rate and design parameters which are for the original Al bonding pads to prove whether the mechanism is proper or not. And these parameters are the opening length of PSG S and polyimide film P, and width of conductor layers M. As shown in Fig.11 in the case of S=100um, it is possible to avoid Al bonding pad corrosion if P=80 um was adopted by preventing the Ti etchant into the Al bonding pad. And if the parameter P was 100um or 90um, there exsisted some Al bondind pad corrosion. Therefore the design parameters have the following relations in this structure

M>S>P=80 um



P : Polyimide film opening width
S : PSG opening width
M : Conductor layer width

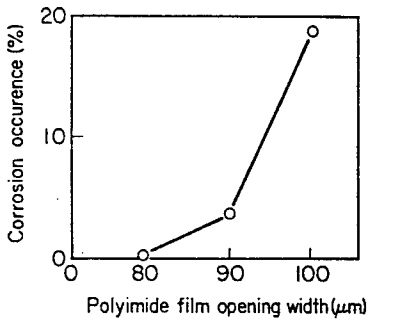


FIG.11 Corrosion occurence rate depending on design parameter

[4] Influence upon device characteristics

Figure 12 shows the NchVth value which is typical for T.E.G. parameters measured during the process. This value equaled the initial value during the process of polyimide film formation and plasma etching. This value shifts out of the definite value during the conductor metal formation process. This phenomenon may be caused by radiation damage, when conductive matal layer was deposited by E-gun deposition. When the device was annealed at 380°C, the NchVth value shifted into the original value once again. Figure 12 also shows the standby current, typical for AC/DC parameters at the same process steps of the T.E.G. parameters. This shifted down a little as the process progressed through the steps but there was no problem for normal operation. Other T.E.G. and AC/DC parameter values do not shift during each process step.

[5] Probing the rearranged pads

Table 7 shows the difference between the AC/DC parameters measured for the Al bonding pads and on the rearranged pads. The measurement values were mean values for 10 chips which were selected 2 chips each at 5 points in one wafer. Comparing the measured values for the Al bonding pads and those for the rearranged pads, no differences and no problems in the specification were found. This result shows that the post-processed devices can be used as LSI chips for high density memory modules.

TABLE 7 AC/DC parameter difference between Original Al bonding pads and rearranged pads

Symbols	Original Al bonding pad			Rearranged pad		
	(V_{DD}) 4.0V	5.0V	6.0V	(V_{DD}) 4.0V	5.0V	6.0V
IDDS(μA)	0.460	0.674	1.096	0.456	0.674	1.094
IDDO(mA)	22.70	33.30	41.96	23.53	35.08	42.98
tACC(nS)	87.80	60.02	54.20	88.00	60.40	55.80
tCO (nS)	92.00	62.40	54.60	92.40	63.40	55.80
tOE (nS)	65.50	38.70	31.00	65.60	38.90	31.00
V_{DD} Max.(V)	2.72			2.72		
V_{DD} Min.(V)	9.310			9.270		

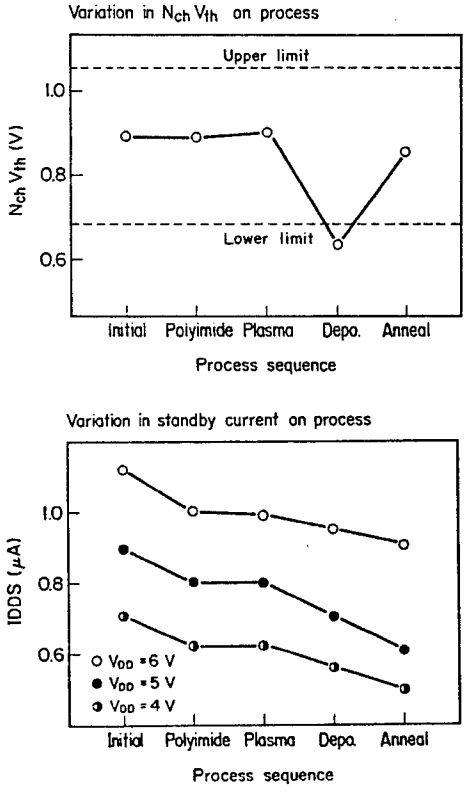


FIG.12 Device characteristics affected by process

[6] Reliability test

The results of tests carried out in accordance with the conditions for the reliability test and defect criteria mentioned above are listed in Table 8. Although the strict criteria for the environment test and life test are established on the basis of the above-mentioned maximum rates, there were no device degradaitions beyond the defect criteria. Each device maintained stable properties, which indicate high reliability of the device.

It is also necessary to check how the electrical properties change or how the range of values for the entire samples change, even if they are within the defect criteria, with the passage of time in the life test, and also before and after applying each environment stress in the environment test. There were no defects in the AC/DC parameters and T.E.G. parameters with the passage of time. Figure 13 shows a result typical for these two parameters showing their changes in value with time in the reliability test.

TABLE 8 Reliability test result for new device

60% confidential level

Test items	Conditions	Sample q'ty	Test time	Total test time, 60% F_a=0 λV	No of defective	Percent defective (%/10^3 hour)
High temperature operation test	T_a =125°C V_{DD} =6.0V	10	1000H	0.95×10^6	0	0.096
High temperature storage test	T_a =150°C	86	1000H	32×10^6	0	0.003
High temperature high humidity storage test	T_a = 85°C RH=85%	85	1000H	—	0	—
High temperature bias test	T_a =125°C V_{DD} =6.0V	10	1000H	0.95×10^6	0	0.096
Temperature cycle test	-55°C (30) -25°C (5) 150°C (30) 25°C (5) one cycle	54	300cycle	—	0	—

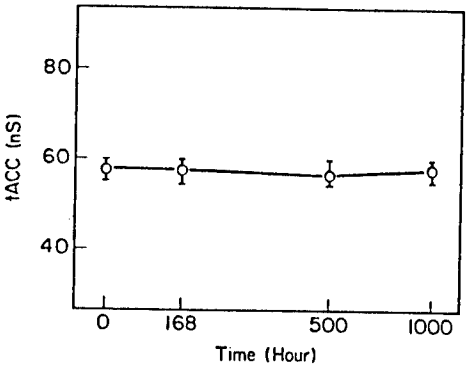


FIG.13 Periodic variation in address access time by high temperature storage test

[CONCLUSIONS]

A new LSI chip was developed in which bonding pads were rearranged suitably for high density packaging. Conclusions are as follows.

(1) Some polyimide residue remaining on the Al bonding pad surface caused an abnormal resistance between the Al bonding pads and contact metal layers. This residue was able to be removed when plasma etching was carried out. Plasma etching is an effective method to remove the polyimide residue from the Al bonding pad.
(2) Ti(1000A)/Ni(3000A)/Au(5000A) was used as conductive metals, because Ni causes sufficient barrier to avoid Al-Au intermetallic compounds.
(3) The design parameters for the polyimide insulating layer and conductive metal layer was established as follows, to obtain high process yields.

M>S>P=80um, if S=100um

(4) The NchVth value, which is one of the device characteristics will be changed easily by radiation damage. However, it is possible to return this and other characteristics to their normal values by annealing. And other T.E.G. or AC/DC parameters did not change their values during the process.
(5) Comparing the AC/DC parameter measurements for the Al bonding pads and for rearranged pads, no difference was found between them in the specification and there was no problem. This result shows that the post-processed devices can be used as LSI chips for high density memory modules.
(6) There were no device degradations beyond the defect criteria, and no defects with the passing of time in the AC/DC parameters and T.E.G. parameters from the results of tests carried out in accordance with the conditions for the reliablity test and defect criteria. Each device maintained stable properties, which indicates high reliability of the device.

[ACKNOWLEGMENT]

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CHIP-ON-GLASS TECHNOLOGY FOR LARGE CAPACITY AND HIGH RESOLUTION LCD

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ABSTRUCT

We have developed the COG (Chip On Glass) technology for large capacity and high resolution LCD. Recent advances in lap-top computers have increased demand for LCD displays with full color capacity, increased resolution and more pixels. Additionally , LCD packaging requires a fine pitch packaging method. We have developed COG to meet the requirements.

In the COG structure , the IC is bonded directly to the glass substrate by means of interconnections between Al pads on the IC and corresponding electrodes on the panel. Electric conductive particles are placed between the pads and the electrodes. The Al pads IC have the following specifications : size 8.80×5.82mm; pad size 102×100μm; minimum pad pitch 134μm; 185 I/O pins. The IC was bonded directly to the panel in a face down position. The IC and the panel were fixed using an adhesive, which results in the easy replacement of faulty IC. The wiring pattern of the ITO electrodes at the connecting area were plated with Ni. Additionally, the input lines were plated with Au. The effect of these steps was to lower the resistivity of the input lines.

We have developed a full color LCD module using this technology with approximately 12 inch diagonal, and 640×3(R,G,B)×480 dots, with a pattern pitch of 130μm. 24th driver ICs are packaged 12 to a side on the top and bottom edges of the module.

1. Introduction

Recently,Liquid Crystal Display(LCD) has been widely found for applications in display terminals of business machines, word processor, PC (personal computer), OA (office automation), TV (television), AV (audio visual). Several measuring equipments needs to be made thinner, lighter weight, and lower power supply. Because there has been a great demand for LCD with improved display quality, high density, large capacity display, and there is very thin in pitch of LCD pattern.

TAB (Tape Automated Bonding) technique is now a popular technology for LCD assembly. The pitch of outer leads is about 200μm. When increasing number of LCD dots and density, the pitch becomes about 100μm, and tape manufacturing becomes very difficult. For the solution of these problems, COG technology, which is the technology of assembling bearing chip directly on LCD panel, has become indispensable.

There are some problems of COG technology now, such as long time spent for bonding and preparation for special IC's and etc.. The problems forced the technology use Wire Bonding, Face Down Bonding with Au bumped ICs. So we have developed the new COG technology, which is the solution of several problems and also is lower in cost and high in reliability.

2. Structure

In the COG technology, the IC is bonded directly to the panel in a face down position. Figure 1 shows the structure of the COG packaging technology which is developed by us. It is necessary to have 13mm in length from the edge of the panel for bonding ICs, shown Fig.1. It is possible to scale to down less than 10mm for the packaging area, if the specific IC is applied to it. Flexible Printed Circuit is connected on the panel with Anistropic Conductive Films to connect the panel to the circuit. The bonding method of the IC are as follows.(Fig.2)

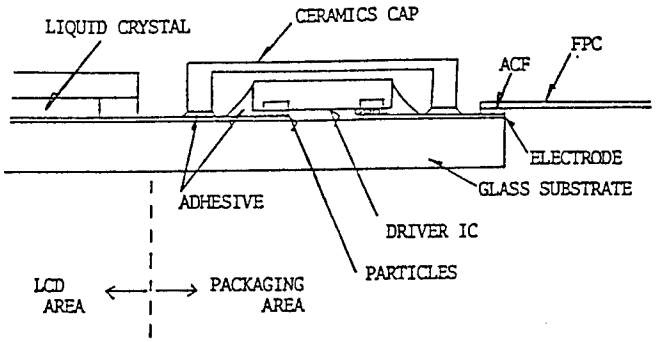

Fig.1 Structure of the Chip On Glass technology

3. Experiment

1) Decrease of the resistance at input line

The input resistance of the driver IC should be reduced to about 0.2Ω/□, but in

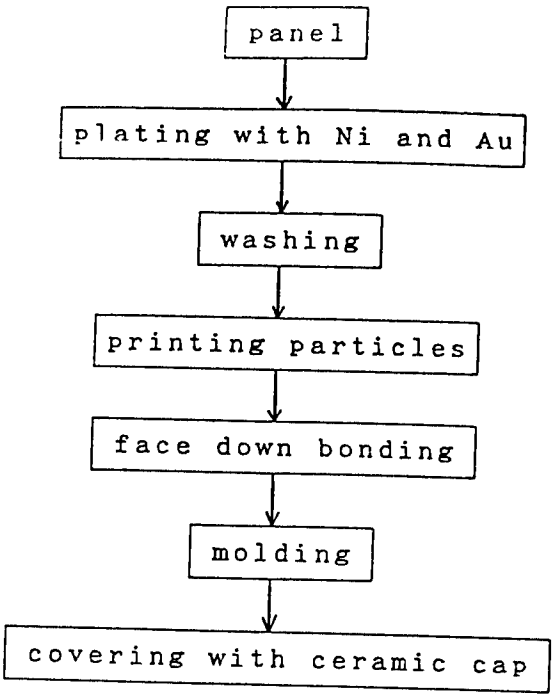

Fig. 2 Process of COG

the case of COG we use ITO line as the input line that has more resistance value than we are required as the input line. The resistance of ITO on the panel is 15 Ω/□ at least. This value of resistance may cause the prolongation of the rise time. In order to reduce the resistance of ITO input lines, we plated Au/Ni on the ITO input lines. The thickness of Au/Ni is about 1000/3000Å, and the sheet resistance is reduced to 0.2Ω/□.

2) Connection between IC pads and the LCD panel

We use a ordinary Al pads IC in stead of a Au bumped IC. By using a ordinary Al pads IC, it is possible for us to apply COG technology to various kinds of ICs and get ICs at lower price than that of Au bumped IC.

As a conductive particle, it should restore to the original state after the compression, and should have very little deviation in diameter. Actually, we have chosen the metal coated resin ball as a conductive particle. Its diameter is 7.5μm with the range of ±1μm.

Table 1 shows the maximum current and the maximum voltage. Fig.3 shows the way to test the maximum current and the maximum voltage.

We have defined the maximum current and the maximum voltage as the voltage and the current that break conductive balls.

From Table 1 , Au-coated resin balls can do 3 times as much current as Ni-coated resin balls. Therefore we select Au-coated resin balls as conductive particles.

3) Repairability (Replacement of the device)

There are 24 bonded ICs on each LCD panels, therefore the repairbility of the IC is indispensable to such a multichip packaging.

We examined the repairbility of the bonding which required thermosetting type and thermoplastic type adhesive.

Fig.4 shows the way to replace the IC.

First, press the tool to a faulty IC and heat the tool to 400℃.

Next, after the adhesive becomes fragile with heat, press the faulty IC from its side and slide and remove it.

In evaluating the replacement method mentioned above, it is found that the both type of the adhesive that has good repairability and easy to replace the ICs.

4. Reliability

To prevent the LCD panel from the heat damage, we have developed a low temperature packaging process as we described and ensured the reliability of the packaged LCD panel.

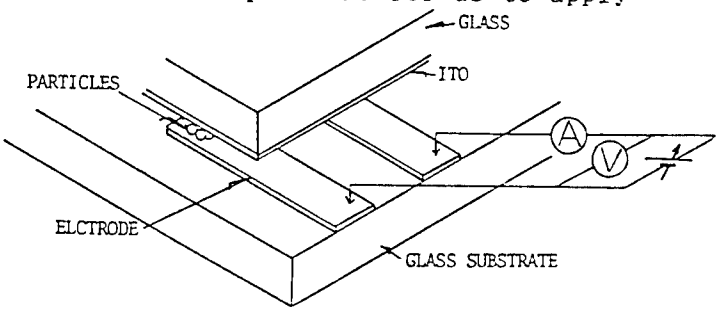

Fig.3 Test circuit of maximum current and maximum voltage

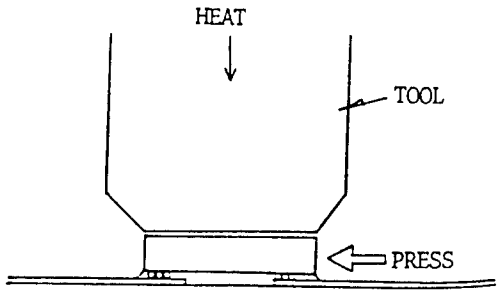

Fig.4 Cross-section view of replacement process

Table 1 Results of the maximum current and maximum voltage

coating metal	thickness (Å)	particles's diameter (φ μm)	maximum current (m A)	maximum voltag (V)
Ni	500	7. 5	66. 8	28. 7
Au	500	7. 5	179. 5	55. 2

1) Packaging structures and adhesives

To compare the reliability, two kind of packaging structures and adhesives were tested. It is mentioned in Table 2.

The packaging structure with a ceramic cap is shown in Fig.6 and that with no-cap is shown in Fig.5.

Table 2 shows that a combination of the ceramic encapsulated structure and thermosetting adhesive results in best reliability.

The cause of the faulty was the invading of moisture to Al pads through a boundary between the adhesive and the panel. The moisture that reach Al pads made the connection open. The thermosetting adhesive provided more resistance against the moisture. The ceramic cap was found to be very effective barrier against the moisture. Therefore we chose the ceramic encapsulated structure with the thermosetting adhesive.

2) Bias humidity test

In order to evaluate the reliability of COG panel (the structure is shown Fig.6), a Bias humidity test was carried out.

Table 3 shows the results.

Now, there is no faulty until 500 Hours. The test is continued.

Table 2 Results of the reliability test (85 ℃ , 85 %RH)

adhesive	hours / structure	0	60	100	150	300	500
thermoplastic resin	with cap	0/5	0/5	0/5	0/5	5/5	-
↑	no-cap	0/5	0/5	3/5	5/5	-	-
thermosetting resin	with cap	0/5	0/5	0/5	0/5	0/5	0/5
↑	no-cap	0/5	0/5	0/5	0/5	5/5	-

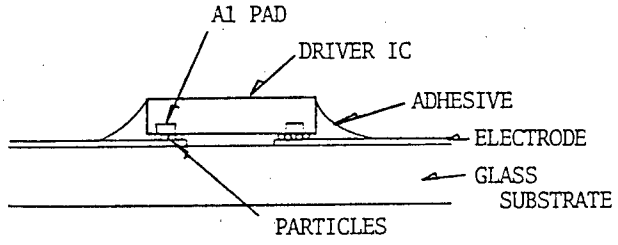

Fig.5 COG STRUCTURE (no-cap)

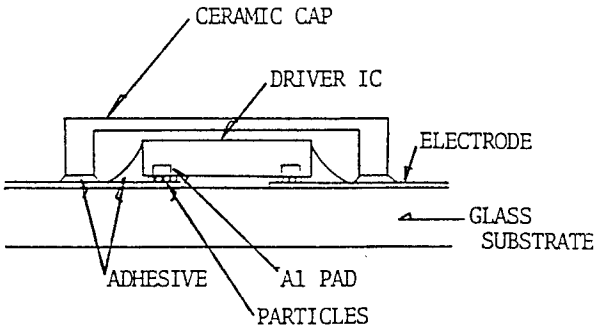

Fig.6 COG STRUCTURE (with cap)

Table 3 Results of the bias humidity test (50 ℃ , 90 %RH , 25V)

adhesive・structure ＼ hours	0	60	150	300	500	-
thermosetting resin・with cap	0/20	0/20	0/20	0/20	0/20	continue

5. Conclusion

We assembled a 12 inches color panel module. The out look of the panel are shown in Fig.7 and Fig.8. Specifications of the panel and the driver IC are shown in Table 4 and Table 5.

We packaged 24 ICs on the panel with COG technology. Other 8 ICs were packaged with TAB technology. This panel was exhibited at Electronics Show held at Harumi, Tokyo in 1988.

The COG technology has made it possible to bond 130μm pitch connections correctly. In the future we will improve the reliability of the adhesive and the cost of packaging vigorously.

Table 4 Specification of the panel

size	12inches
liquid cristal	NTN
driving method	multiplex-addressed with 16harmonies
dots	640×3(R,G,B)×480
duty	1/240
pattern pitch	SEG : 130μm (COG) COM : 390μm (TAB)
driver IC	SEG : SED1760×24 (COG) COM : SED1704× 8 (TAB)

Table 5 Specification of the driver IC (SED 1760)

output lines	160
frequency	16MHz
output voltage	max 40V
size	8.80×5.62mm
pad pitch	134μm
others	4bit,16harmonies

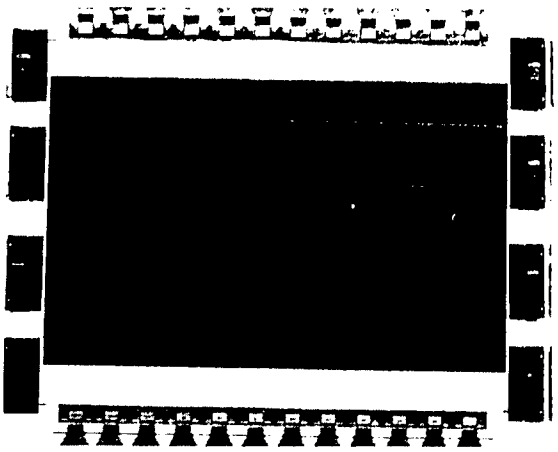

Fig.7 24 ICs are assembled by COG and 8ICs by TAB.

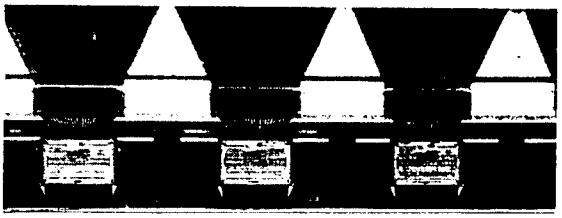

Fig.8 Assembled ICs by COG

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2) H.Yoshida,Y.Tagusa,K.Inada,A.Kawashima ,H.Makita, Y.Dotta, S.Nakabu and K.Awane, "Packaging method of liquid crystal driver LSIs by Tape-On-Panel technology", ISHM 1988 Proceedings, p.307-313, 1988

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A NEW PACKAGING FOR DIP TYPE THICK FILM HYBRID IC

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ABSTRACT

This paper discusses a new packaging method for DIP type thick film hybrid IC's presently used in digital electronic exchange equipment. This method has replaced previous packaging methods due to its economy and high reliability. It was also introduced with the objective of automation. The new packaging uses a structure consisting of a dam component and a filler component of silicone resin. Thick film hybrid IC's packaged with this silicone resin showed good resistance properties after 1000 hours of 90 degrees C, 90% relative humidity, 175 VDC bias testing. In addition, the bonding resistance between substrate and parts was unchanged after 100 cycles of a -25℃ to +85℃ heat shock test. This new packaging technology has been production of thick film hybrid IC's used in digital electronic exchange equipment, giving good results with no adverse effect whatsoever in the market to this date.

INTRODUCTION

With the miniaturization and high integration of the LSI circuit, the thick film hybrid IC has come into more demand as a highly functional, highly reliable module. In the past, hermetic sealing processes using inert gas injection were often used to achieve the necessary high functionality. Just with advances in high-purity of resins in recent years, simple, low-cost resin sealing methods have become more popular. The main resin sealing methods are cast molding and immersion. Table 1 summarizes the major types of packaging methods.[1] [2] The nature of the immersion process limited it to the SIP (Single Inline Package), with the problem that after sealing the resin layer could be uneven. Cast molding could be used in either SIP or DIP (Dual Inline Package), but the process was complicated by the need for a degassing operation to remove air bubbles residual between the case and the hybrid IC. Also, there was the structural problem of increased weight. This paper discusses a highly reliable packaging technology for thick film hybrid IC's with ceramic substrates, developed to eliminate the problems of other methods and achieve increased automation in a resin sealing process. Samples of packaging with silicone resin, epoxy resin and phenolic resin were prepared, and the reliability of each was evaluated. We further discuss the search for an automated packaging method capable of quick adaptation to a future variety of versatile thick film hybrid IC applications, and the achievement of a sealing method that protects the reliability of exchange equipment modules manufactured by mass-production processes.

Table 1. Packaging Methods

	Sealing Method	Sealing Materials
Hermetic Seal	Low Melt Point Glass Method	Borosilicate Lead Glass Borosilicate Zinc Glass
	Soft Wax-Method	Gold-tin, Gold, Silicon Gold-germanium
	Welding Method	Cobalt Nickel
	Resin Adhesive Method	Epoxy Resin
Resin Seal	Local Packaging Method Local Packaging Method	Thermo-set Silicone, Epoxy, Phenolic Resin
	Cast Molding Method	Thermo-set Epoxy, Silicone Resin, Silicone Resin Gel
	Immersion Method	Thermo-set Silicone, Epoxy, Phenolic Resin
	Transfer Mold Method	Thermo-set Epoxy Resin

EXPERIMENTAL

3.1 Preparation of Resin Evaluation Samples

Three types of resin material were used; silicone, epoxy and phenolic. Each was evaluated for resistance to humidity and heat shock. Two types of silicone resin, condensing and additive, were selected. Also, epoxy resins of different Cl^- ion density were used. A liquid phenolic resin was chosen chosen and its effect on various properties was studied. Of the basic properties of the resins used, viscosity, linear expansion and Cl^- ion density are shown in Table 2.

Table 2. Resins Evaluated

Property \ Type	Silicon		Epoxy		Phenolic
	A (condensing)	B (additive)	C	D	E
Viscosity (P)	6	80	30	120	60
Linear Expansion Coefficient x 10^{-6} (1/℃)	200	210	27	23	5
Cl^- ion Density (ppm)	8	10	150	1000	1

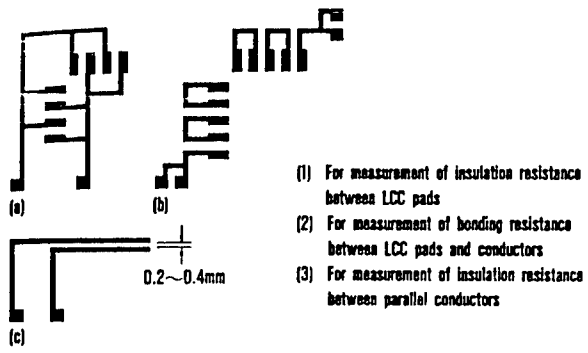


Fig. 1 Test pattern Example

Table 3. Test Conditions

Item evaluated	Test	Conditions	Time	Quality measured
Humidity resistance	① HHBT		1000^{H}	Insulation resistance
	② PCT		100^{H}	Insulation resistance
Heat shock test	③ HST		100^{C}	Bonding resistance
Overall reliability	④ Combined	③+②+①	$100^{C}+100^{H}+1000^{H}$	Insulation resistance

order. It was also determined to measure trimming resistance by the same method.

3.3 Investigation of Automated Resin Packaging

Automated packaging was investigated using the silicone resin, which produced the best results in the above tests.

Table 4. Humidity Test Results

Insulation resistance measurement location	Test No.	Silicone		Epoxy		Phenolic
		A	B	C	D	E
Parallel conductors	①	1	1	1	1	1
	②	1	1	1	1	1
	④	1	1	1	1	1
Between lead terminal connection pads	①	1	1	2	2	1
	②	1	1	2	3	1
	④	1	1	3	3	1
Between LCC pads	①	1	1	2	2	1
	②	1	1	1	2	1
	④	1	1	2	2	1

1: $\geqq 10^{10}$ ohms
2: 10^{8} to 10^{10} ohms
3: $<10^{8}$ ohms

A 60 mm x 40 mm 96% alumina substrate with a Pd/Ag conductive paste and RuO_2 resistive paste was used for evaluation. A humidity resistance evaluation pattern and a heat shock resistance evaluation pattern were printed and baked on to the substrate. The humidity resistance evaluation pattern consisted of parallel conductors separated by 0.2, 0.3, 0.4 mm gaps, 0.8 mm gap lead terminal connection pads, and a pad pattern loaded with an 0.6 mm gap LCC (Leadless Chip Carrier), so that the insulation resistance between the parallel conductors and pads could be measured. The heat shock resistance evaluation pattern was configured with pads for lead terminal connection, and an LCC loaded pattern with trimming resistance, so that changes in the bonding resistance between the lead terminal and the LCC, and in the trimming resistance could be measured. Test pattern examples are shown in Figure 1. After the LCC for insulation resistance measurement (1) and the LCC for bonding resistance measurement(2) were loaded onto the substrate and leads attached to the terminals, the samples were packaged with each type of resin and used for evaluation.

(1) An empty LCC without IC bonding.
(2) A LCC without IC bonding, but with 1 pin each connected so that bonding resistance could be measured.

3.2 Methods for Resin Evaluation

Evaluation consisted of HHBT (High temperature, high humidity bias test), PCT (Pressure cooker test), HST (Heat shock test), with changes measured before and after in each factor of reliability, as shown in Table 3. It was determined to measure humidity resistance between the parallel conductors and between the lead terminal bonding pads, as well as between the LCC pads attached for insulation measurement, using an insulation meter in the range of 10^{7} ohms to 10^{11} ohms. Heat shock resistance was measured by reading the bonding resistance of the lead terminals and the loaded LCC for bonding resistance measurement, using the 4-terminal method on the milli ohm

RESULTS AND DISCUSSIONS

4.1 Resin Evaluation

Table 4 shows the Humidity Test results under each test condition for silicone resin, epoxy resin, and phenolic resin. The results are classified with the numeral 1 for passing grades when insulation resistance of 10^{10} ohms or more was maintained, 2 for greater than 10^{8} but less than 10^{10} ohms, and 3 for failure, less than 10^{8} ohms.

All resins showed good results of 10^{8} ohms or higher with no deterioration in insulation resistivity in tests①, ② and ④ between parallel patterns and between LCC loaded pads. No difference attributable to the difference in the silicone hardening reaction was seen. However, in the insulation resistance between lead terminal connection pads, the epoxy showed deterioration. As shown in Figure 2, sample C, which had Cl^{-} on density in excess of 1000 ppm frequently fell below 10^{8} ohms in test ④, the combined test. The epoxy resin was peeled off and failure analysis performed. Figure 3 shows the results of element analysis of Pd and Ag by the EPMA surface analysis method between pads. The lead terminals corroded and the presence of Ag, the structural metal of the conductor, was confirmed between the pads. This can be thought to have been caused by peeling in the interface between the lead terminal and the epoxy resin surface during the heat shock test, with moisture penetrating into the peeling area under high temperature and humidity, resulting in the removal of Cl^{-} ions.

Next, the results of heat shock test evaluation are shown in Figure 4. Epoxy resins C and D both showed more than $\pm 10\%$ variation in bonding resistance and cracks appeared in the resin surface. Other resins showed less than $\pm 2\%$ change and were outstanding in resistance to heat shock.

The above testing showed that the resins best suited to our objectives were the silicone and phenolic resins.

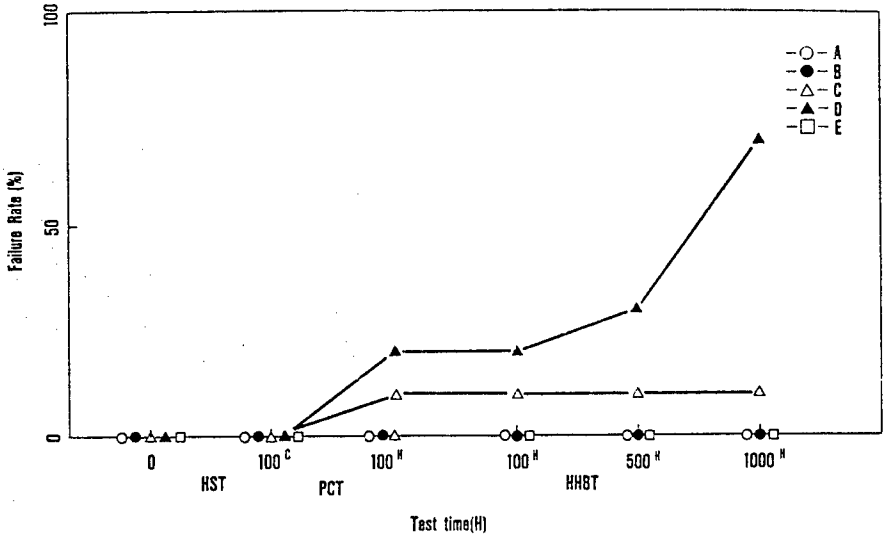
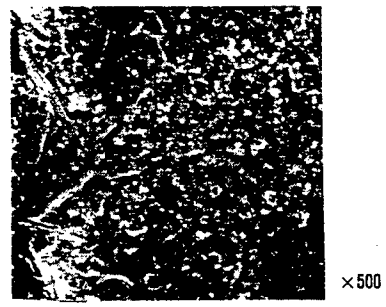


Fig. 2 Failure Rate of $10^8\Omega$ or Lower Insulation Resistance in Combined Test ④



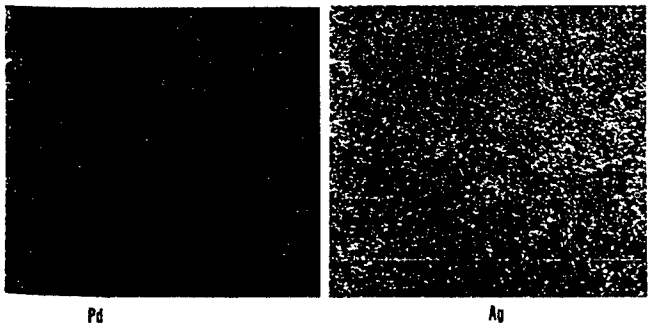


Fig. 3 SEM/EDX Observation of Lead Terminal Pad Intervals

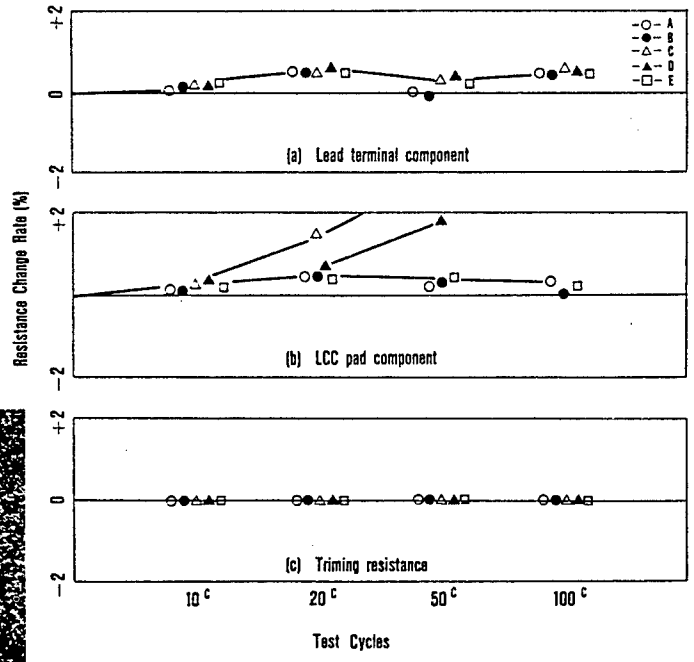


Fig. 4 Change of Resistance in Heat Shock Test ③

Table 5. Sealing Method Study

Sealing Method	Number of Processes	Related Member	Adaptation to Different Substrate Shapes	External appearance	Cost	Overal Evaluation
Cast Molding Method	4	Cast	Cast Change	Good	High	No Go
Immersion Method	3	—		Bad	Low	No Go
One-Sided Sealing Method	2	—		Average	Low	Go

Table 6. Silicone Resins for Automation Study

Quality	B	B_1	B_2
State	Thixotropic	Fluid	Non-fluid
Viscosity (P)	80	35	3000
Linear Expansion Coefficient x 10^{-6} (1/℃)	210	200	210

Table 7. Additional Testing Items

Test Item	Quality Tested	Test Method Test Method	Result Result
Adhesion	Shear Hardness	18mm x 10mm x 1mm adhesive section drawn at 10mm/min	3.7 kgf/cm² Cohesive failure coefficient 100%
Flame Resistance	Combustion Interval	Glow wire method 960℃/30 sec.	0.1 sec.
Hardening Stoppage	Hardness	Soldering flux added and hardness measured	Partial change
Solvent Resistance	Hardness	Hardness measurement Surface inspection	No change No change

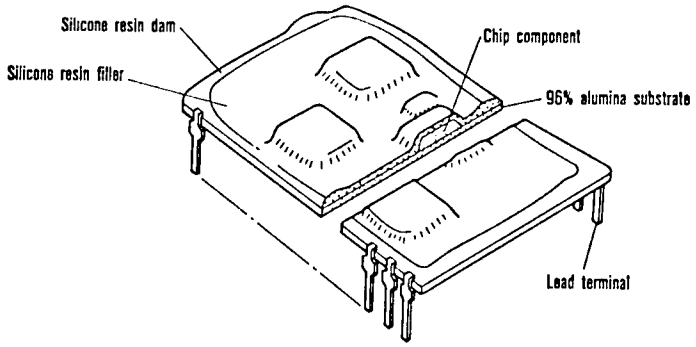


Fig. 5 Packaging structure

4.2 Investigation of Automated Packaging

In order to select a sealing method and a resin suited to automation, a study was made of sealing techniques, including the cast molding and immersion methods in use up to the present, and the one-sided sealing method that we have considered using as a new technique. The standards for evaluation were principally the case of the sealing process, low cost, and case of adaptation to various kinds of substrates. The results of the evaluation are shown in Table 5.

The cast molding method requires a special cast for each substrate shape, and has related problems in increased weight and treatment of the air bubbles that get in between the substrate and the cast. The immersion method has high variability in the thickness of the resin layer. In view of the above, it was determined that one-sided sealing with resin extruded from a dispenser would be the most suitable. Between the silicone and phenolic resins, it was decided that the easily-handled additive type silicone resin B would be used because it creates no by-products during hardening, and its heat-controllable hardening time makes it well-suited to automation. Because condensing-type silicone reacts with moisture in the air and begins to harden, on the other hand, by-products are created and hardening quality in substantial depth area is poor. Its hardening time of 8 to 16 hours is quite long and difficult to control.[3]

Phenolic resin has complex hardening conditions requiring an air drying process for 2 to 4 hours before hardening, and was excluded because this did not suit it to automation.

At this point, two more types of Resin B with differing viscosities, B_1 and B_2, were prepared, and the three types were tested as shown in Table 6.

Additional testing of uses of Resins B, B_1, B_2 was performed shown in Table 7, to verify that there were no problems with reliability.

Specifically, the packaging structure, shown in Figure 5, consists of a dam portion and a filler portion of silicone resin. The dam portion is required to adhere to the substrate and lead terminals and to be able to form a leakproof seal with the end face of the substrate. To meet these requirements, the silicone resin must have the proper viscosity and thixotropy and maintain a thixotropy that will prevent leakage even during the viscosity changes of thermal hardening. For this reason we measured the viscosity changes of the three resins at different temperatures from room temperature up to 100 ℃. As shown in Figure 6, each of the resins reached its lowest viscosity around 80℃.

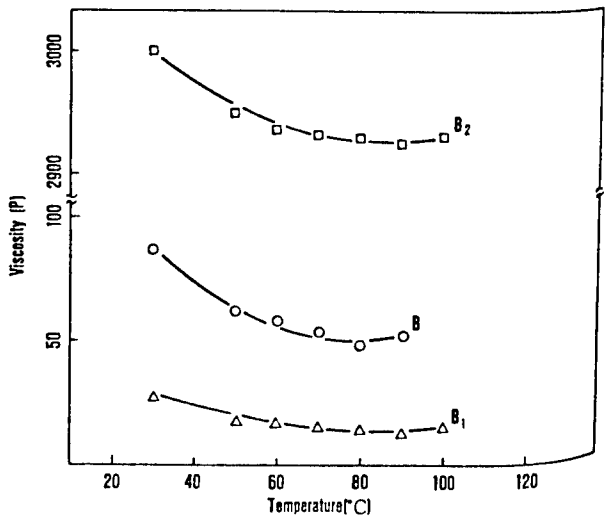


Fig. 6 Temperature —Viscosity Correlation of Silicone Resins B.B_1.B_2

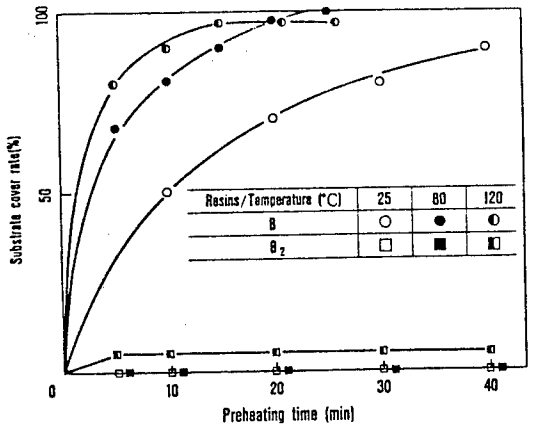


Fig. 7 Relation Between Preheating Temperature, Time and Coverage Rate of Silicone Resins B and B_2

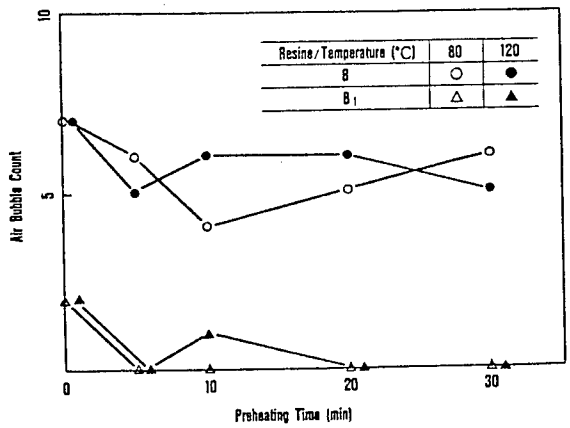


Fig. 8 Relation Between Preheating Temperature, Time and Air Bubble Count Per Unit Area of Silicone Resins Band B_1

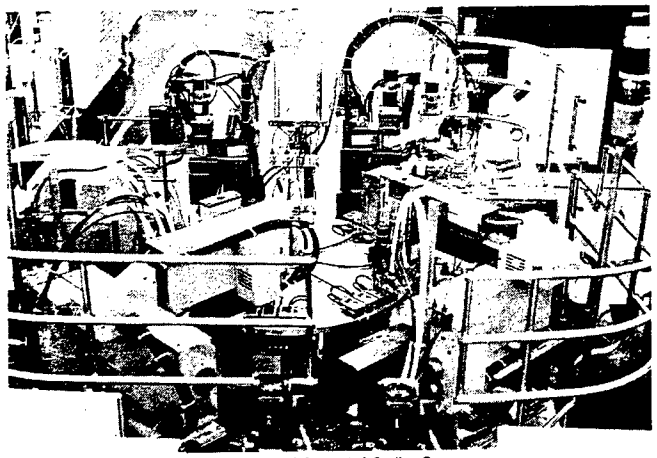


Fig. 9 Design of Automated Sealing Process

Table 8. Overview of Hybrid IC's

No.	Type	External Dimensions (mm)	Application
1	DIP	60.6 x 37.8 x 3.7	General, Common Telephone SLIC*3
2	DIP	55.0 x 27.6 x 3.7	Public Telephone SLIC
3	DIP	65.0 x 21.0 x 3.7	Optical Transmission Module

*3: SLIC (Subscriber Line Interface Circuit)

Figure 7 shows the results of our study of the effects of preheating on the sealing capacity of resins B and B_2 (excluding the fluid B_1). Sealing capacity is expressed as the substrate coverage rate of when the resin was extruded about 2mm inside of the edge of the substrate. In this test resin B, after 30 minutes of preheating at 80℃ at which it reaches its lowest viscosity, achieved a 100% coverage rate and formed a perfect dam.

Next, the filler component is required to completely cover the loaded components with little intrusion of air bubbles and a good external appearance. Excluding the non-fluid resin B_2, resins B and B_1 were tested for preheating conditions and residual air bubbles, and the results are shown in Figure 8. Residual air bubbles were expressed as the count of air bubbles per unit of surface area after the resin over the LCC loaded components was peeled off and the residual air bubbles in the resin were counted. It was discovered that preheating resin B_1 at 80 ℃ for 10 minutes eliminated residual air bubbles.

As a result, the packaging process was designed as follows.

(1) Resin B was extruded from a dispenser onto the end surface of the substrate forming a dam, and the dam was saved in unhardened state.

(2) Next, resin B_1 was deposited from a dispenser to fill in the area inside the dam.

(3) The sealing capacity of both dam and filler was enhanced by preheating for 30 minutes at 80℃ and with the residual air bubbles minimized, the unit is sent into the main hardening process.

With the above process design, complete automation could be achieved by combining the dispensers for the dam and filler components, supply robots and a continuous curing oven. Also, by simply changing the extrusion from the dispenser, (needle diameter, pressure, movement rate, position, etc.) the system could accomodate different substrate shapes.[4] Figure 9 shows the automated equipment for this process.

4.3 Application to Thick-film Hybrid IC's for Exchange Equipment, and Reliability

This new packaging technology was suited to the high reliability and high productivity demands of the thick-film hybrid IC for exchange equipment. An overview of types, etc. of hybrid IC's is given in Table 8.

For local exchanges, functional operation for 20 years in environmental conditions of between 10℃ and 40℃ (temperature increase of 30℃) is considered basic. In order to obtain good transmission quality, the hybrid IC's for these exchanges must satisfy more than 30 digital and analog properties. The reliability standard established for for the thick-film hybrid IC to be able to satisfy these conditions is shown in Table 9.[5]

No defects attributable to resin packaging have been disclosed by these tests.

Further, in the five years since mass production of thick-film hybrid IC's was begun, not one failure in the market has been experienced.

Table 9. Thick-film Hybrid IC Standards

Test Item		Conditions	Standard
Property Evaluated	Insulation Resistance	JIS C502 7.3 page (DC100V)	10^8 ohms or greater
	Insulation Pressure Resistance Resistance	MIL-STD-20-2-2E-30 (DC500V 1 min) DC resistance measurement by 4-terminal method	0.5 mA or less within ± 2%
	Film Adhesion Hardness	2mm square pad measurement	average 400g/mm² or greater
Environment Test	Heat Cycle Test	-25℃ to +85℃ 100 cycles (JIS C5030)	
	High Temperature Shelf Test	85℃ 1000H (3000H) (JIS C5022 adapted)	
	High Temperature High Humidity Self Test	60℃ 90% RH 1000H	–
	Heat & Humidity Cycle Test	175V 40 cycle (MIL-STD-202E-106D)	
	Other	Active Aging Test 60℃ 168H	

CONCLUSION

As discussed above, it was found that for humidity resistance and heat shock resistance, the best packaging materials for thick-film hybrid IC's with ceramic substrates were silicone resin and phenolic resin. Additive-type silicone resin was found to be the easiest to handle in application of automation. By selecting two additive-type silicone resins of differing viscosity and thixotropy, automation of a highly reliable packaging structure composed of dam and filler components was achieved, and it became possible to speedily adapt to substrates of different shapes.
This packaging technology has been introduced in the manufacturing process of thick-film hybrid IC's for exchange equipment, and is now in stable mass production. In the future, we would like to continue the effort to develop new packaging technologies in order to reach higher levels of quality and economy.

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HIGH-ACCURACY INNER LEAD BONDING TECHNIQUE

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ABSTRACT

Miniaturizing electronic apparatus requires the interconnection of high pin count IC dies to finely pitched leads. However, conventional wire bonding can hardly meet this requirement. Recently, the tape automated bonding (TAB) technique has been employed to achieve high pin count and high density packaging.

A fully automated inner lead bonder has been developed. Using this newly developed machine, bonding accuracy and bond strength have been investigated. The obtained results indicate that the bonding accuracy is good and that the bonding condition range is wide.

This technique has been applied for LCD module mass production.

INTRODUCTION

Miniaturizing electronic apparatus and increasing the number of I/O terminals requires interconnection of high pin count IC dies to finely pitched leads.

However, it is getting difficult for conventional wire bonding to meet this requirements because of wide pad spacing and high wire loop. The gang bonding technologies, TAB and flip chip, has been suggested as the next level of IC's packaging and chip joining processes to replace wire bonding.

Fig.1 shows schematic diagrams of TAB process. A fully automated inner lead bonder has been developed which simultaneously bonds all inner leads on tape to gold bumps on an IC die after completing the high accuracy tape to die alignment. By using this newly developed machine, bonding accuracy and bond strength have been investigated.

The inner lead bonder and the bonding technique are mentioned below.

INNER LEAD BONDER

An external view and a diagram of the newly developed inner lead bonder are shown in Photo.2 and Fig.2.

The machine is operated as follows. Carrier tape, mounted on the tape loader, is fed to the bonding stage at constant pitches by the driving sprocket wheel. Then, a CCD camera takes pictures of the inner leads on tape at two points.

On the other side, an IC die is picked from the wafer station and placed onto the bonding stage by a pick-and-place unit. The IC die on the stage is aligned by the gauging unit and the pattern on the IC die, determined by the CCD camera, is also recognized at two points.

The tape-to-die alignment is accomplished correctly for X, Y and θ directions. Then, the constantly heated tool simultaneously presses all inner leads into the gold bumps on the IC die. ILB operations are repeated in sequence.

The charasteristic performance for this machine is as follows.

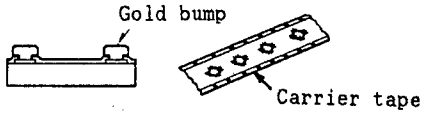
(1) High-accuracy alignment
The alignment accuracy has been achieved to 9.3 μm ($3\sigma_{n-1}$).

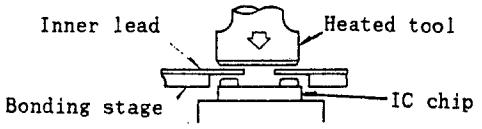
(2) High-speed bonding
The index time for this machine is 2.9 seconds without bonding time.

(3) Applied for 35 and 70 mm wide tapes
35 and 70 mm wide tapes can be used with standerd, wide, and super wide types of sproket holes.

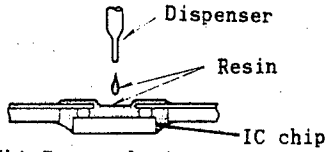
(4) High bonding pressure
Maximum bonding pressure is 30 kgf, produced by an air cylinder.

(5) Easy set-up
The bonding tool has a standard face to adjust at right angles.

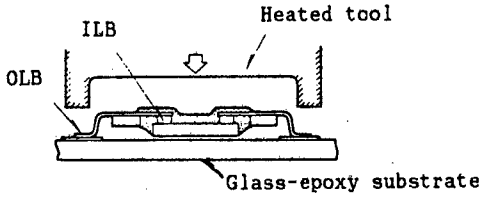




(a) Inner lead bonding (ILB)



(b) Encapsulation



(c) Outer lead bonding (OLB)

Fig. 1 TAB process

Table.1 shows specifications for this machine.

Table. 1 Specifications

Items	Specifications
Tape width	35,75 mm
IC size	3~12 mm
Accuracy	10 μm
Index time without bonding time	2.9 sec/die
Bonding pressure	0.5~30 kgf
Die supply	wafer:6" tray :4"
Machine Size	1600W×1200D×1680H

This machine was developed with strict attention paid to the alignment accuracy. The high alignment accuracy was achieved by adopting the following construction; (A) The inhouse recognizing apparatus, which has a recognition accuracy of 3.5 μm for tape and 2.5 μm for an IC. (B) Precision X-Y-θ tables, which have 2 μm resolution and 0.0075 degree per pulse. (C) The two points recognizing system, which recognizes two individual points on tape and an IC die, and calculates the position error for X,Y and θ.

The alignment error defined in Fig.3 was measured at four points on an IC. The measurment was repeated fifty times, using the same IC die and inner leads. Table.2 shows the alignment accuracy for this machine. Accuracy better than 10 μm ($3\sigma_{n-1}$) was obtained.

EXPERIMENTAL RESULTS AND DISCUSSION

By using this machine, the following subjects are investigated; (A) Appropriate bonding conditions. (B) Bonding accuracy. (C) Bond strength transition. (D) Bonding reliability.
Results are mentioned below.

Appropriate bonding conditions

First of all, the relation between the bond strength and the bonding temperature at the surface of the bonding tool has been investigated in regard to some bonding pressures. IC dies having 182 I/O terminals with 140 μm pitch and 90 μm square gold bumps were mainly employed in this experiment. Table.3 shows the main specimens used.

Table. 2 Alignment accuracy

Average	0.5	(μm)
$3\sigma_{n-1}$	9.3	(μm)
Max.	10	(μm)
Min.	-4	(μm)

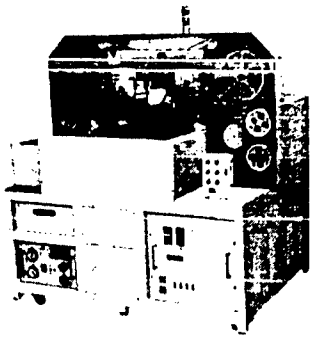


Photo. 1 Inner lead bonder exterior view

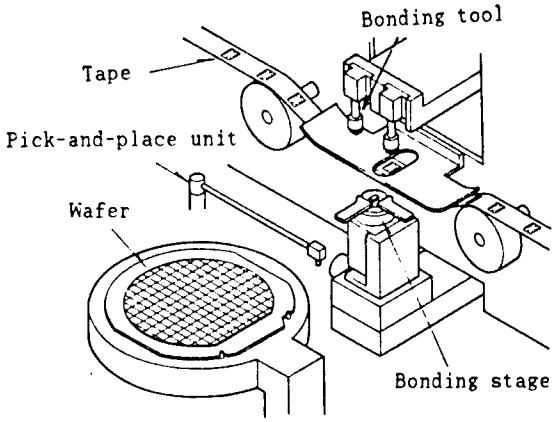


Fig. 2 Inner lead bonder diagram

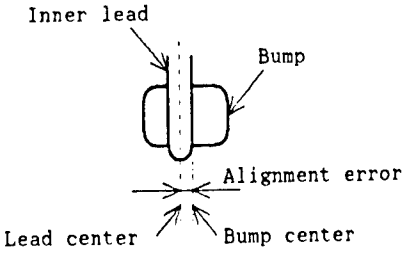


Fig. 3 Alignment error measurement

Table. 3 Main specimens

IC size	5×9.5	(mm)
Bump size	90	(μm)
Bump hight	24	(μm)
I/O terminals	182	
Tape width	70	(mm)
Inner lead width	60	(μm)
Inner lead thickness	35	(μm)

The bond strength was estimated by the pull test, as shown in Fig.4. It is more than 30 gf over 400 ℃, irrespective of the bonding pressure. However, the melted state of tin plated on copper leads has a little difference, as shown in Photo.2. The heat and pressure form the gold-tin eutectic bond at the interface between gold bumps and tin plated copper leads. At 350 ℃, the bond strength becomes weak and the inner leads are peeled off from the bumps because of insufficient reaction.

The relation between the bonding time and the bond strength has been investigated, too. The results indicate that, at over 400 ℃, high bond strength is obtained, even in 0.3 second bonding time. However at 350 ℃, the bond strength is poor, and it can not be improved by increasing bonding time. Under all bonding conditions, no damage appeared on the chip passivation film or the silicon itself.

From the above, it is clear that 450 ~ 500 ℃ bonding temperature, 50~70 gf/pad bonding pressure and 1 second bonding time are the appropriate bonding conditions.

Bonding accuracy

In this paper, the alignment accuracy and the bonding accuracy of inner leads to gold bumps have a different meaning. The alignment accuracy means the machine's capacity, but the bonding accuracy is influenced by the error in the tape configurations. Therefore, the bonding accuracy is usually worse than the alignment accuracy. Table.4 shows the bonding accuracy results. Good bonding accuracy ($3\sigma_{n-1}$) of 13.5 μm was obtained for IC dies by this bonder, as shown in Table.4.

To study the allowance limits for the alignment error, test samples, which were bonded intentionally shifting the bonding position, were made. Fig.5 shows the relation between bond strength and bonding accuracy.

The bond strength does not drop so much as the bonding accuracy becomes worse. However the alignment error reaches 25 μm, the bumps are peeled off from the electrodes by the pull test. Observing the section of the interface having 30 μm error, it is clear that the gold bump is crushed on the chip passivation film (Photo.3). Therefore, over 25 μm error should be avoided in this sample. Tests on the bonding accuracy show that the maximum error is 13.6 μm . Therefore, this machine's bonding accuracy is good enough to bond IC dies having 184 I/O terminals with 100 μm pitch and 60 μm square bumps to 40 μm wide inner leads, as shown in Photo.4.

Table. 4 Bonding accuracy

Average	1.5	(μm)
$3\sigma_{n-1}$	13.5	(μm)
Max.	13.6	(μm)
Min.	-4.9	(μm)

IC dies: 122 I/O terminals with 132 μm pitch and 90 μm square gold bumps
Leads : 60 μm wide

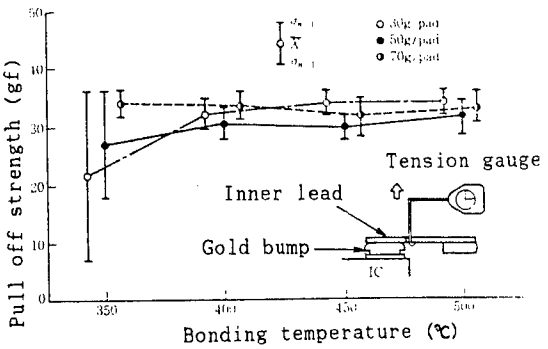
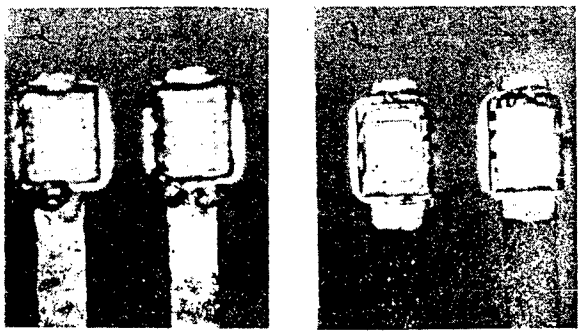


Fig. 4 Relation between temperature and bond strength



at 400 (℃) at 500 (℃)

Photo. 2 Tin melting

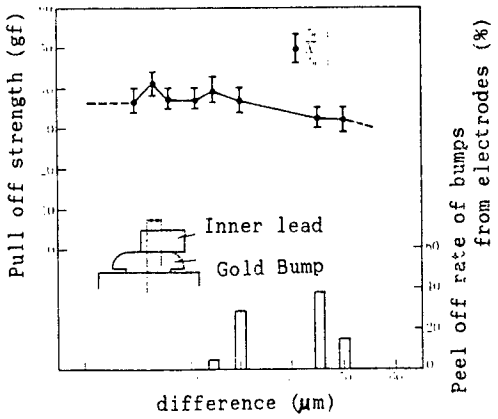
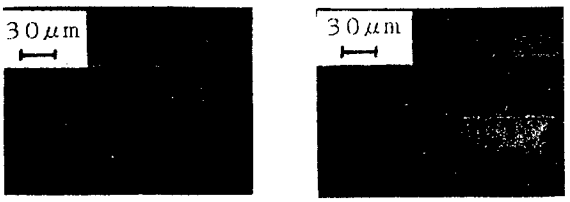


Fig. 5 Relation between bonding accuracy and bond strength



Difference:2 (μm) Difference:30 (μm)

Photo. 3 Cross-section of bonds

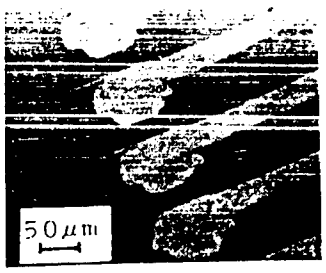


Photo. 4 SEM micrograph of bond

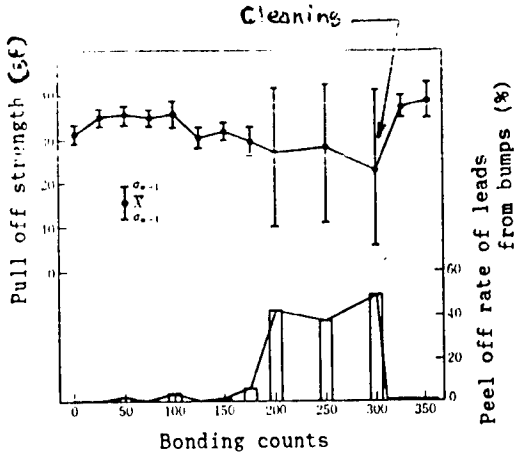


Fig. 7 Relation between bonding counts and bond strength

Table 5 Reliability test

Test items	Test conditions
High temperature storage test	Ta=100℃, t=1,000hrs
High temperature and high humidity storage test	Ta= 70℃, RH=90~95%, t=1,000hrs
Low temperature storage test	Ta=-40℃, t=1,000hrs
Thermal shock test	Ta=-40℃~100℃, N=100cycle
Pressure cooker test	Ta=121℃, P=2atm, t=48hrs

Mass productivity and reliability

The relation between the bonding counts and the bond strength is shown in Fig.6. At over 150 bonding counts, the bond strength becomes unstable. At the same time, the failure rate at the interface between leads and bumps is increased. This is because the tin oxide, which adheres on the surface of the bonding tool, makes heat conduction insufficient. This machine is equipped with a cleaning unit to remove the tin oxide from the bonding tool surface. It is evident that the bond strength recovers by using the cleaning unit after 300 bondings. In mass production, the bond strength is stabilized by cleaning the bonding tool every 100 times.

Reliability tests, indicated in Table.5, were carried out. Satisfactory results were obtained on the bond strength or electric characteristics.

CONCLUSION

A high-accuracy inner lead bonder has been developed to achieve high pin count and high density packaging. This machine has been applied for LCD module mass production etc.

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DEVELOPMENT OF TFT-LCD TAB MODULES

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ABSTRACT

The authors have developed 4" and 6.5" diagonal a-Si thin film transistor active matrix liquid crystal displays (TFT-LCD) modules by means of tape automated bonding (TAB) technology. The small frame size, i.e. 12.5 mm for 4" modules, has been realized by using U-shape bending tape carriers. In the inner lead bonding (ILB) process, the Au bumps on a driver LSI are connected with the Cu/Sn inner leads on a tape carrier by high speed and fully automated gang bonding technique. The LSIs are encapsulated with halogen ion free epoxy resin. In the outer lead bonding (OLB) process, the Al electrodes on an LC panel are connected with the outer leads on a tape carrier through anisotropic conductive film (ACF) by thermocompression apparatus. The ACF, which consists of thermosetting resin and dispersed Ni particles, realizes the highly reliable OLB. The TFT-LCD module reliability was confirmed by various environmental and mechanical tests.

1. INTRODUCTION

Recently, TFT-LCD modules have been intensively developed. The compact module structure is especially required for portable TV use. The key points in the TFT-LCD module technology are as follow:

1) Module design technology
2) Interconnection technology

The TAB technology, using S-shape bending tape carriers, was reported (1) for 3" TFT-LCD modules. Although it realizes compact TAB modules, the structure is still complicated. The authors have developed simple 4" and 6.5" TFT-LCD TAB modules. Small frame sizes were obtained by using U-shape bending tape carriers.

For TFT-LCD TAB modules, high density packaging and fine pitch interconnections are also required. The authors have developed a high speed, fully automated inner lead bonder (2). By using this machine, a highly productive inner lead bonding (ILB) technology has been established. The highly reliabile outer lead bonding (OLB) between Al electrodes and Cu/Sn leads was also developed by using highly reliable anisotropic conductive film (ACF).

This paper describes the module structure, interconnection technology, and the results of reliability tests. The 4" TAB modules are described in detail, since there is no significant difference between 4" and 6.5" module techniques.

2. 4" TFT-LCD MODULE STRUCTURE

The external appearance of the module is shown in Fig.1. Figure 2 shows a cross sectional view of the bending part of a tape carrier. Specifications for 4" TFT-LCD modules are shown in Table 1. The frame size has been minimized to 12.5 mm.

The LC panel has 480 source electrodes and 220 gate electrodes, covering 105,600 pixels. The module has four X-driver LSIs and two Y-driver LSIs. The X-driver LSI has 18 input electrodes and 120 output electrodes. The Y-driver LSI has 7 input electrodes and 120 output electrodes. Au bump pads are fabricated on each LSI. The Au bumps on a driver LSI are connected with inner leads on a tape carrier by gang bonding technique. The Al electrodes on an LC panel are connected with outer leads on a tape carrier (output terminals) by using ACF. The X-side OLB lead pitch is 250 μm and the Y-side lead pitch is 230 μm.

Input pads on a driver LSI are also connected with inner leads on a tape carrier (input terminals). The tape carrier input terminals are connected with electrodes on a printed circuit board (PCB) by soldering. Chip parts and a control IC are also mounted on it.

3. MANUFACTURING PROCESS OF TAB MODULES

Key processes in TAB technology are interconnections. ILB and OLB are important elements in the TAB technology.

3.1 ILB PROCESSES

A Driver LSI, with 23 μm thick Au bumps, was joined on a 70 mm wide tape carrier. The tape carrier used is as follows. Polyimide film, which has low thermal expansion, is 75 μm thick. Cu leads 35 μm in thickness are laminated on the polyimide film by glue. Sn layers 0.4 μm in thickness are formed on Cu leads.

ILB is implemented by Au-Sn eutectic bonding between Au bumps and Cu/Sn leads. The Au atom diffusion into the active area is blocked by barrier metal layers. On the other hand, Sn penetrates into the Au area, and Au-Sn eutectic layers are formed. Next, chip coating follows. The resin employed is halogen ion free.

There are 180 interconnections between inner leads and driver LSI Au bump pads. The inner lead pitch is 140 μm. ILB conditions were determined by mechanical and metallurgical evaluations.

Optimum conditions are as follow:

1) Bonding temperature range is between 450 ℃ and 500 ℃.
2) Bonding pressure range is between 50gf/pad and 70gf/pad.
3) Bonding time is approximately 1 second.

The pull off strength for each inner lead was more than 30gf/lead.

3.2 OLB PROCESSES

Al electrodes on an LC panel are connected with Cu/Sn leads on a tape carrier through an ACF. It realizes a lump interconnection of multi-terminals at low cost and in a short time. The OLB process reliability is more important than the ILB process. The reason is that OLB is carried out mechanically, while ILB involves a metallurgical process.

Evaluation samples were fabricated which consisted of a tape carrier and Al electrodes on a glass substrate. These samples were examined under high temperature and high humidity test (80 ℃ , RH 95%, 1000 hr). Thermosetting type ACF was selected which had the highest reliability. Ni particles approximately 5 μm in diameter were dispersed in the thermosetting resin film. A cross sectional microphotograph of the OLB interconnection area is shown in Fig.3. The constant heat bonder was employed for OLB.

Optimum OLB conditions are as follow:

1) Bonding temperature is 170 ℃.
2) Bonding time is 20 seconds.

By using this ACF, four X-side tape carriers with LSIs and two Y-side tape carriers with LSIs were connected with the LC panel, as shown in Fig.1.

3.3 TAPE CARRIER BENDING AND SOLDERING TO PCB

The tape carriers connected with the LC panel are bent into a U-shape, as shown in Fig.2. Input terminal leads for driver LSIs are soldered to the electrodes on a printed circuit board (PCB), where chip parts and a control IC are mounted. The pulse heat bonder was employed for this soldering process.

4. RELIABILITY TEST RESULTS

Reliability was examined for three kinds of test samples, i.e. ILB, OLB, and modules. The test conditions are summarized in Table 2.

4.1 ILB RELIABILITY

Tape carriers with LSI chips were examined by storage tests, as shown in Table 2. To evaluate the reliability, the contact prober system was introduced. Input signals were supplied to the input terminals and output signals were measured at all output pads. The results are shown in Table 3. The numerical designations in Table 3 represent the number of no-good samples per total number of test samples. All samples showed normal performance after these storage tests.

4.2 OLB RELIABILITY

Glass substrates with patterned Al-Cr electrodes were employed as dummys. The outer lead pitch was 230 μm. All pair Al-Cr electrodes on a glass substrate are shorted at the end of the electrodes.

Connection resistances were measured with a digital multi-meter. The test samples were examined by various environmental tests, and results were compared with the initial resistance values. Figure 4 shows the connection resistance changes at each pair pad position, during the high temperature and high humidity storage test. The changes in connection resistances after 1000 hours were within 1 ohm. Figure 5 shows the average connection resistance change values for 63 pair pads during the high temperature and high humidity storage test. The test samples were also examined by storage tests, as shown in Table 2. The results of these tests are shown in Table 3. There was no pad with an open connection or short. Similar results have been obtained by other environmental tests. It has been proved that the present OLB interconnection system has high reliability.

4.3 TFT-LCD MODULE RELIABILITY

Various environmental and mechanical tests, shown in Table 2, were also introduced for 4" TFT-LCD modules. The module reliability was evaluated by comparing the picture with the initial state. There was no increase in defects, such as line defects, or point defects, during these tests. The results are shown in Table 3.

5. CONCLUSION

TFT-LCD TV modules were developed by using U-shape bending TAB technology. These modules were examined by various environmental and mechanical tests. It has been proved that these modules have high reliability. The characteristics for the present modules are as follows:

1) The highly productive and highly reliable ILB has been obtained by gang bonding between inner leads and Au bump pads.
2) The frame size for an LC panel has been minimized by using U-shape bending tape carriers.
3) The highly reliabile interconnections between LC panel electrodes and outer leads on a tape carrier

have been achieved by using ACF consisting of Ni conductive particles and thermosetting resin.
4) Developed TFT-LCD TAB modules also have high reliability.

6. ACKNOWLEDGMENT

The authors wish to express their thanks to Dr. T. Shimada, Dr. Y. Oana, Mr. E. Suzuki, and Mr. K. Kasahara for their support and suggestions in carrying out this development.

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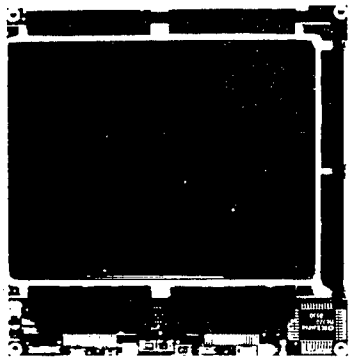

Fig.1 4" TFT-LCD Module

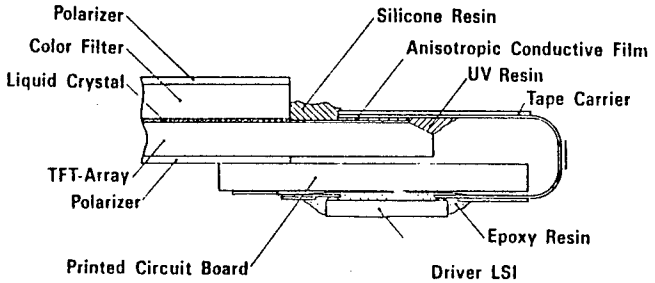

Fig.2 LCD Module Cross Sectional View

Table 1 LCD Module Specifications

Items		Contents
Display Size (inch)		4
External Dimensions (mm)		108(W)x105(H)x5.2(D)
Display Area (mm)		80.6x60.5
LC Display Mode		Twisted Nematic
Driving Method		TFT Active Matrix Addressing
Pixel Number		480x220
Driver LSI	: X-Driver	120 out x 4p
	: Y-Driver	120 out x 2p
Connection Pitches (μm)		250(X), 230(Y)

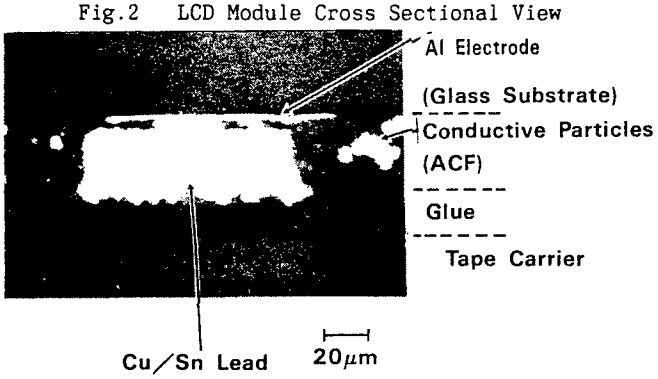

Fig.3 OLB Connection Cross Sectional View

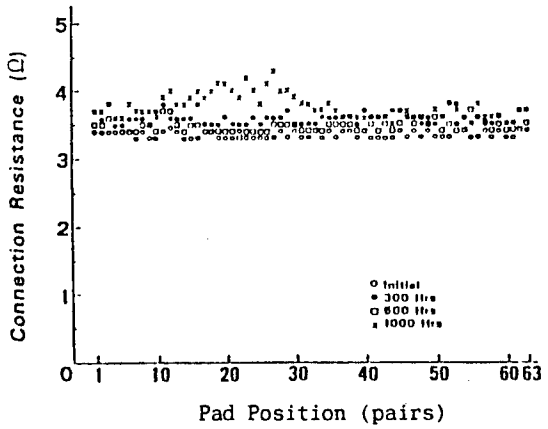

Fig.4 High Temperature and High Humidity Storage Test (70℃, RH 95%) Results at Each Pair Pad Position

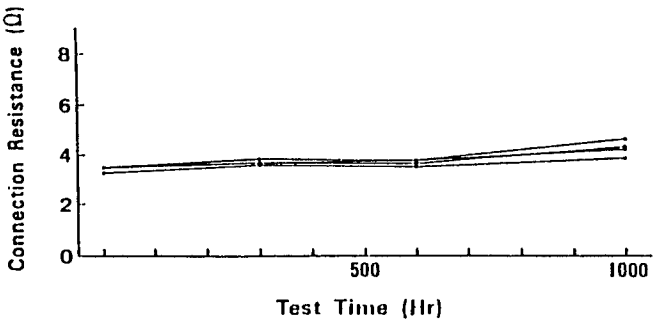

Fig.5 Average Value Changes for Connection Resistances during High Temperature and High Humidity Storage Test (70℃, RH 95%)

Table 2 Reliability Test Conditions

Test Items	Module	OLB	ILB
Room Temperature Operation Test	RT. 1000Hr	—	—
Intermittent Operation Test	RT. 1000Hr On-30min~Off-30min	—	—
High Temperature and High Humidity Operation Test	65°C, RH 95%, 1000Hr	—	—
High Temperature Operation Test	80°C, 1000Hr	—	—
Low Temperature Operation Test	-30°C, 1000Hr	—	—
High Temperature and High Humidity Storage Test	65°C, RH 95%, 1000Hr	70°C, RH 95%, 1000Hr	70°C, RH 95%, 1000Hr
High Temperature Storage Test	85°C, 1000Hr	100°C, 1000Hr	100°C, 1000Hr
Low Temperature Storage Test	-40°C, 1000Hr	-40°C, 1000Hr	-40°C, 1000Hr
Temperature Cycling Test	-30°C~85°C, 100 cycles (1Hr/cycle)	-40°C~100°C, 100 cycles (1Hr/cycle)	-40°C~100°C, 100 cycles (1Hr/cycle)
Temperature and Humidity Cycling Test	-10°C~25°C~65°C, RH 95% 10 cycles (24Hr /cycle)	-10°C~25°C~65°C, RH 95% 10 cycle (24Hr /cycle)	-10°C~25°C~65°C, RH 95% 10 cycle (24Hr /cycle)
Pressure Cooker Test	—	—	2atm, 121°C, 48Hr
Shock Test	100 G x 6 ms. Direction: x,y,z	—	—
Vibration Test	10≠500 Hz,1.5 mm or 10 G Direction: x,y,z	—	—

Table 3 Reliability Test Results

Test Items	Module	OLB	ILB
Room Temperature Operation Test	0/3	—	—
Intermittent Operation Test	0/3	—	—
High Temperature and High Humidity Operation Test	0/3	—	—
High Temperature Operation Test	0/3	—	—
Low Temperature Operation Test	0/3	—	—
High Temperature and High Humidity Storage Test	0/3	0/3	0/3
High Temperature Storage Test	0/3	0/3	0/3
Low Temperature Storage Test	0/3	0/3	0/3
Temperature Cycling Test	0/3	0/3	0/3
Temperature and Humidity Cycling Test	0/3	0/3	0/3
Pressure Cooker Test	—	—	0/3
Shock Test	0/3	—	—
Vibration Test	0/3	—	—

A NEW FACE DOWN BONDING TECHNIQUE USING A LOW MELTING POINT METAL

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ABSTRACT

Recently, many kinds of fine pitch bonding techniques have appeared.

The authors have developed a new face down bonding technique for use in making an LCD (liquid crystal display) panel. The maximum bonding temperature is limited by the heat resistance temperature for the liquid crystal materials and polarizer plates. The bonding temperature is approximately 150 ℃. Using a low melting point metal, such as an indium alloy, the IC electrodes and bonding pads on a glass substrate are connected at a temperature less than 150 ℃. This technique is called the "low melting point metal connection (LMC) technique".

At first, low melting point metal bumps were formed on the IC bonding pads with gold bumps by dipping. Shallow-bowl-shaped bumps, 10 - 20 μm high, were formed by this method. After this bump formation, the IC and the glass substrate were connected. This process was carried out at a pressure of 30 gf/bump or less and at a temperature of 150 ℃ or less.

Using the sample fabricated as mentioned above, two kinds of reliability tests were carried out. One was a thermal shock test (TST; a repetition of -40 and 100 ℃ for 30 minutes each, 300 cycles), and the other was a high temperature and high humidity test (70 ℃, 90%R.H., 500 hours). Stable results were obtained for both tests.

Finally, dot matrix LCD panels, with 640 × 400 dots, were assembled with 20 driver IC chips. They worked well.

The LMC technique makes it easy to test the IC bonds and to repair them in case of any defect.

This LMC technique can be applied to LCD panels and many other kinds of electronic equipments.

1. INTRODUCTION

The bare chip assembly technology has great importance in high density and minimized assembly of electronic devices.[1][2] Since the IC electrodes become multi-pin with a fine pitch, a technique for connecting the electrodes and conductive patterns should be further developed.

Recently, LCDs (liquid crystal displays) are becoming popular in various display applications. They are considered to obtain a large market share in the future, instead of cathode-ray tubes. Because an LCD has a large number of picture elements, its driver ICs have to supply many signals corresponding to the number of individual picture elements[3]. Therefore, the COG (chip on glass) technique, which can be used to mount ICs directly on the LCD panel, in the form of a flip chip, has been developed.[4] The maximum bonding temperature is limited by the heat resistance temperatures for the liquid crystal materials and polarizer plate, which are generally approximately 150 ℃. However, the conventional flip chip method is not applicable for assembling driver ICs on the LCD panel, because the heat resistance temperature for the LCD panel is not high enough for the solder bump melting point.

As a COG technique method, the authors have developed a new face down bonding technique for LCD panels. Using a low melting point metal, such as an indium alloy, the driver IC electrodes and conductive patterns on the glass substrate can be connected at a temperature less than 150 ℃. This is called the "low melting point metal connection (LMC) technique".

This paper describes the bump formation method, the results of experimental bonding, reliability test and trial manufacture of 640 × 400 dot matrix LCD panels with 20 ICs mounted on each.

2. LMC TECHNIQUE OUTLINE

The LMC technique consists of the following processes, as shown in Fig. 1. Figure 2 shows a schematic cross-sectional view of a connection, using the LMC technique.

(1) Produce low melting point metal bumps on the gold bumps on the IC bonding pads.
(2) After aligning of the conductive pattern on the LCD panel with these bumps, press and connect at less than 150 ℃.
(3) Test the performance for each IC.
(4) Impregnate resin into those products which have passed the test and cure the resin. Products which failed the test must be repaired.
(5) Carry out the final inspection for the LCD panel.

3. LMC TECHNIQUE CHARACTERISTICS

The LMC technique features are as follows.

(1) The bonding temperature can be specified at less than 150 ℃, because indium alloys are employed as the low melting point metal. An alloy containing indium is so ductile that it is difficult to break

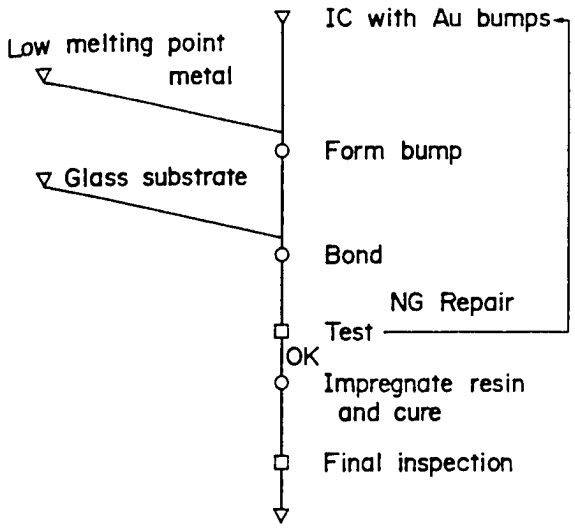

Fig.1 Assembly process block diagram for prototype LCD panel

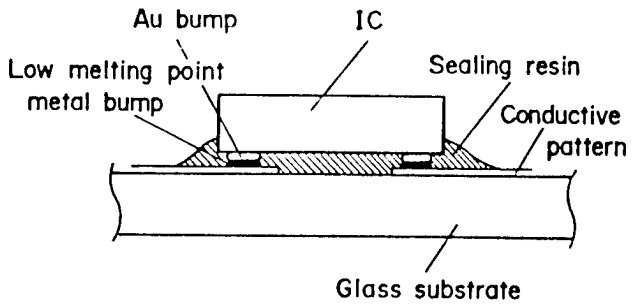

Fig.2 Schematic cross-sectional view of connection for LMC

Table 2 Glass substrate specification

Substrate size	50 x 50 mm
Substrate thickness	1.1 mm
Conductive pattern	ITO / Ni

Table 1 Specification for X and Y driver IC and test IC

	X driver IC	test IC	Y driver IC
Chip size	5.12 x 5.36 mm		5.22 x 6.44 mm
Number of pads	99		117
Minimum pad pitch	162 μm		132 μm
Chip thickness	440 ± 40 μm		
Gold bump height	18 ± 2 μm		
Bump dimensions	85 x 85 μm		

connected portions with thermal shock.
(2) The mounting time for multi-output IC can be reduced, because all terminals can be connected simultaneously.
(3) Mounting cost can be reduced, because of the small quantity of components for assembly.
(4) High density mounting is possible, because of the small connection area.
(5) Repair work is easier.

4. BUMP ELECTRODE FORMATION

Table 1 shows the specification for X and Y driver ICs for an LCD panel, and test ICs, which are used herein. The test IC was manufactured for measuring the contact resistance under the same specification as the X driver IC. Chip sizes for the test IC and X driver IC were 5.12 × 5.36 × 0.44 mm, around which 99 gold bump pads, 85.0 × 85.0 μm in dimensions, were aligned. The minimum pitch for the gold bumps was 162 μm, and the height thereof was 18 ± 2 μm. Aluminum wires for the test IC were connected for every other pad, designed so that the contact resistance could be measured.

On the other hand, the chip size for the Y driver IC was 5.22 × 6.44 × 0.44 mm, around which 117 gold bump pads, 85.0 × 85.0 μm in dimensions, were aligned. The minimum pitch for the gold bump was 132 μm, and the height thereof was 18 ± 2 μm.

The IC chip was precoated with flux, and dipped in a molten indium alloy bath heated to 170 - 200 ℃ for several tens of seconds. The flux reduced and removed the oxide film from the bath surface, so that the indium alloy bump electrodes could be selectively formed only onto the gold bumps on the IC. After electrode formation, the IC was cleaned by an organic solvent, so as to remove the flux and other residua. The indium alloy bumps are shown in Fig. 3. Its cross section is shown in Fig. 4. It can be observed from Fig. 4 that a shallow-bowl-shaped bump was formed on an about 20 μm gold bump. The electrode height was about 30 - 40 μm, including the gold bump height. The bump shearing strength ranged from 50 to 75 gf. It was found that the bump was not separated at the gold bump and indium alloy boundary interfaces.

5. TEST ASSEMBLY ON A GLASS SUBSTRATE

5-1. BONDING EXPERIMENTS

Connections were made between the test IC (refer to Table 1) and the test glass substrate (Table 2). When an actual connection process is considered, a wider range for the connection condition is favorable. This report discusses connection load. A connection load was in the 0.5 - 3.0 kgf range per chip. As the test IC had 99 pads, the connection load per bump reached 1/100, and 5 - 30 gf per bump was obtained.

5-2 RESULTS AND DISCUSSION

Approval or disapproval of these connection conditions was judged by measuring the contact resistance. The resistance was measured using four probes, applying a prober to the test glass substrate.

Fig. 5 presents the relations between the percent defective of connection and contact resistance

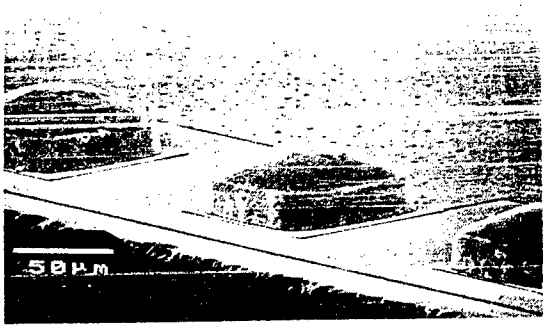

Fig.3 Indium alloy bumps, with SEM

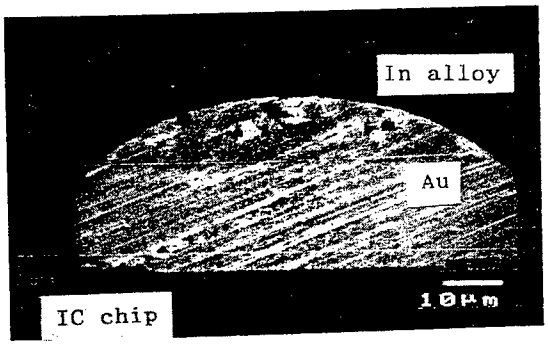

Fig.4 Cross-sectional view of bump with SEM

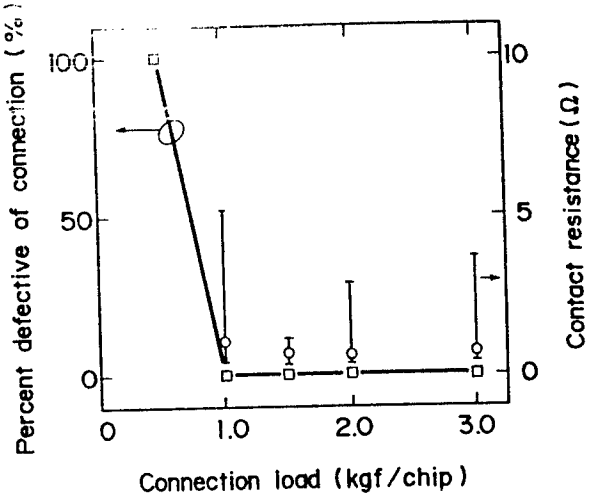

Fig.5 Percent defective of connection and contact resistance versus connection load per IC chip

Table 3 Reliability tests

	Test condition	Cycles or time
thermal shock test	-40/100℃, 30/30 min.	300 cycles
high temperature and high humidity test	70℃, 90 %R.H.	500 hours

versus the connection load per IC chip. When the connection load for the IC chip was 5 gf/bump, the percent defective of connection was high. On the other hand, when the connection load for the IC chip was 10 - 30 gf/bump, the percent defective of connection was low, and a wider process condition range was obtained without a short defect between adjacent bumps. This value causes very little damage to the elements, on the ground that the connection load is lower compared with the traditional wire bonding method or the TAB (tape automated bonding) method. It was also found that the mean contact resistance was less than 1 ohm.

6. RELIABILITY TESTS

Two kinds of reliability tests were carried out as indicated in Table 3. One was a thermal shock test (TST;repeat -40 and 100 ℃ for 30 minutes, respectively) for 300 cycles. The other was a high temperature and high humidity test(70 ℃, 90 %R.H.) for 500 hours.

The TST test results are shown in Fig. 6. The high temperature and high humidity test results are shown in Fig. 7. An epoxy family resin, developed for the LMC, was employed as the sealing resin.

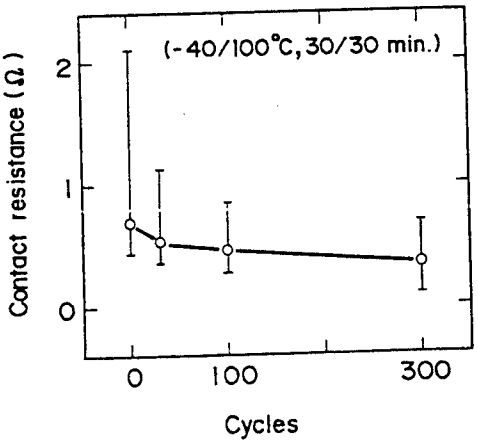

Fig.6 Thermal shock test results

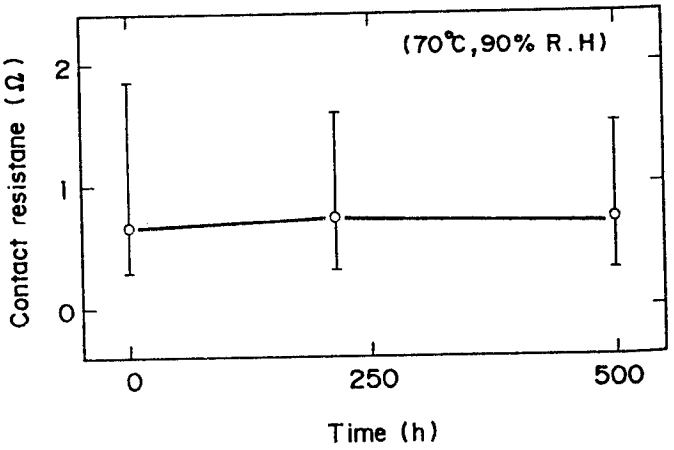

Fig.7 High temperature and high humidity test results

Reviewing these results, it was found that there existed stability in both the TST and the high temperature and high humidity test. Furthermore, it was concluded from those results that the LMC technique can be regarded as a reliable method.

4. TEST ASSEMBLY ON A PROTOTYPE VERY FINE DOT MATRIX LCD PANEL

Prototype tests on very fine dot matrix LCD panels were carried out, based on assemblies on test glass substrates. The dot matrix LCD panels have 640 × 400 dots. The mounted ICs consisted of 16 pieces of the X driver IC, 80 outputs, and 4 pieces of the Y driver IC, 100 outputs. The structure for the conductive pattern of the LCD panel was equivalent to that for the test glass substrate, where nickel pattern is formed on the ITO (indium tin oxide) pattern.

Probing inspection for every IC chip was conducted after mounting. The IC was repaired if there was a connection defect. At this time, the chip could be easily separated. Unless any defect was found during the inspection, a newly developed resin was impregnated and cured. The resin impregnation was quickly accomplished capillary phenomenon.

Power source lines and signal inputs in the LCD panel were connected by an anisotropic conductive film, using an FPC (flexible printed circuit). Figs. 8 and 9 show the prototype LCD panel. An enlarged figure of the connection area appears in Fig. 10.

The test pattern for the display screen appeared throughout the display area, and it could be ascertained whether or not a normal image was displayed on every IC. A normally operating product could be obtained. Fig. 11 shows a display screen for the LCD.

5. CONCLUSION

Results in regard to the LMC technique can be summarized as follows.

(1) A 10 - 20 μm indium alloy bump electrode was able to be formed on a gold bump by the dip method.
(2) Chips could be connected to the nickel pattern at low pressure (30 gf/bump or less) and low temperature (150 ℃ or less). The mean contact resistance was less than 1 ohm.
(3) This technique allows easy testing and repair.
(4) It has been proved through reliability test that the contact resistance did not increase by the TST (repeat -40 and 100 ℃ for 30 minutes each, 300 cycles) and the high temperature and high humidity test (70 ℃, 90 %R.H., 500 hours).
(5) It was possible to obtain prototype operationable 640 × 400 dot matrix LCD panels.

It was verified from above that the LMC technique was applicable to mounting a bare chip IC at low temperature. This method can be applied to LCD panels, and to many other kinds of electronic equipment.

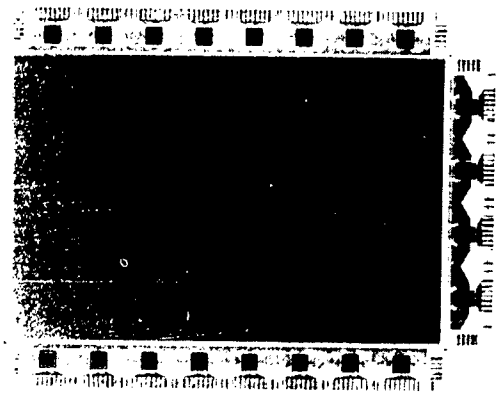

Fig.8 Prototype LCD panel

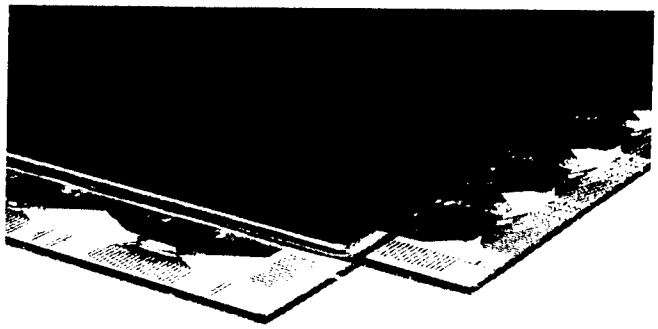

Fig.9 Prototype LCD panel

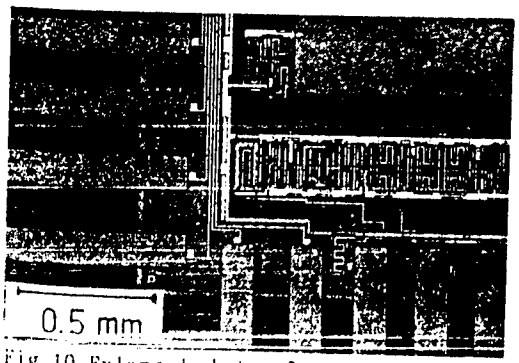

Fig.10 Enlarged photo of connection area

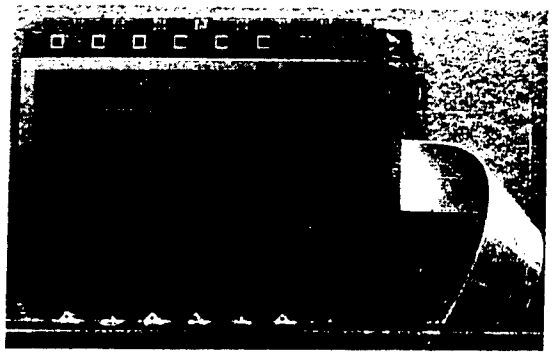

Fig.11 LCD panel display screen

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A PILLAR-SHAPED VIA STRUCTURE IN A CU-POLYIMIDE MULTILAYER SUBSTRATE

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Abstract

This paper describes a new pillar-shaped via structure in a Cu-polyimide multilayer substrate and its novel fabrication process. The process forms a fine rectangular via conductor by pattern electroplating using a thick positive photoresist. Furthermore, a flat polyimide dielectric layer is formed only by the photolithographic process using a photosensitive polyimide precursor. The resulting pillar-shaped via conductor is 30 μm square and 25 μm thick. The area occupied by this via conductor is 25 % smaller than a conventional via not filled with copper conductor, the interconnection density is twice as high, and the thermal resistance is 50 % less. This new via structure is suitable for high-speed signal transmission in a Cu-polyimide multilayer substrate.

Introduction

Steady advances in the speed and integration scale of LSIs have created a demand for higher density packaging to reduce signal transmission delay and thus improve electrical performance. Multilayer substrate packages with low resistivity copper signal lines and a polyimide dielectric layer with a low dielectric constant have been developed for high performance electronic systems.[1)-5)]

In conventional Cu-polyimide substrate packaging techniques, including via fabrication in which copper is deposited on the side walls of via-holes,[1)-3)] the upper via cannot be stacked up on the lower one. Therefore the via conductor occupies a large area in the package and when the via is formed for interconnecting several layers, the signal lines are long.

A pillar-shaped via structure filled with copper conductor has been proposed to overcome these problems.[4)-5)] However, the fabrication process involves mechanical polishing for flattening the polyimide dielectric layer. Mechanical polishing is a complicated and time-consuming process, and the dielectric layer surface may be damaged.

This paper describes a new technique for fabricating a pillar-shaped via. It forms a fine rectangular via conductor using thick photoresist patterning. After photosensitive polyimide precursor coating and prebaking, the dielectric layer surface is planarized by a new photolithography technique instead of by mechanical polishing.

Fabrication Process of New Via Structure

The fabrication processes of the new via structure and the conventional one are compared in Figure 1. (1) A thin copper film is deposited by electroless plating and the first conductor signal line is formed by electroplating. (2) Via patterns are formed in a thick positive photoresist. (3) A copper conductor pillar is built in the via patterns by electroplating, and the positive photoresist and the electroless plated film are removed. (4) A photosensitive polyimide precursor is spincoated and prebaked. (5) After exposure using the new photomask with a continuously varying transparency of the exposure energy, the polyimide precursor is developed and cured to give a thick, flat polyimide dielectric layer. (6) The second conductor signal line is formed. Processes (1) to (6) are repeated to give a multilayer substrate.

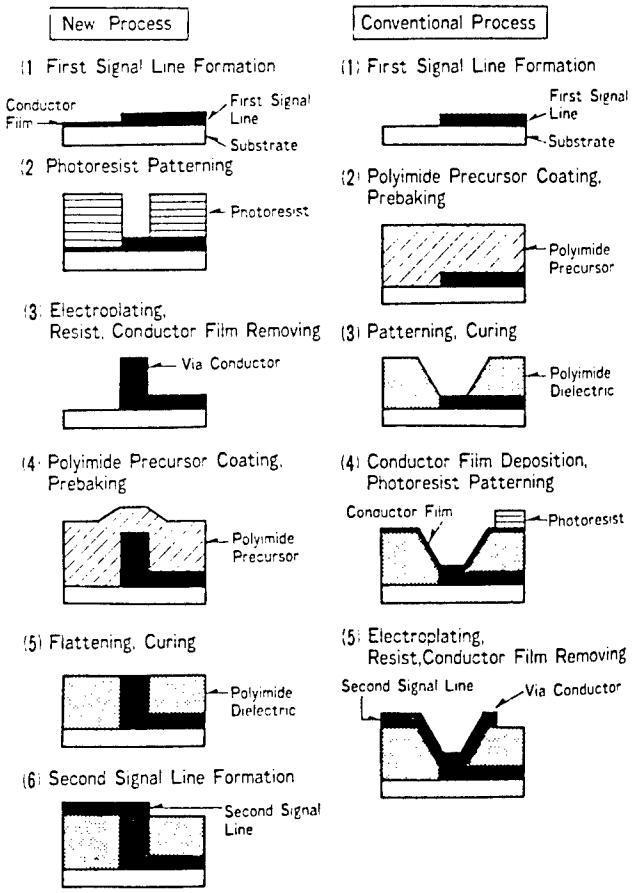


Figure 1 Fabrication process for a multilayer substrate

One feature of this process is the formation of fine, rectangular, high aspect ratio via patterns in a thick positive photoresist, which is about 20 or 30 times as thick as that of an LSI process. In the conventional process, via patterns are formed during polyimide layer formation, so the diameter of the top of the via is about twice the polyimide layer thickness.

The other feature is the formation of the flat polyimide layer by a new photolithography technique. Since the solvent of the photosensitive polyimide precursor evaporates during prebaking, there is a height difference between the dielectric layers on the conductor surface and on the substrate. This height difference was reduced and a flat undamaged polyimide layer was obtained by making use of the property that exposure energy determines the polyimide precursor's solubility in the developer and its configuration during curing. Thus a photomask was used that could control an exposure energy corresponding to the height difference to be reduced.

Experimental Results

(1) Conductor Formation

A fine pillar copper conductor is required for high density packaging. The technical problem is forming a fine rectangular pattern for electroplating using a thick positive photoresist. Careful control of an exposure energy and a development time can obtain the good pattern cross-sections of a thick positive photoresist shown in Figure 2.

After patterning of a photoresist and electroplating, a fine via copper conductor was formed. Figure 3 shows the 30 μm square and 25 μm-thick via copper conductor after the photoresist had been removed. The taper angle between the vertical line and the side of the conductor is about 7 degrees.

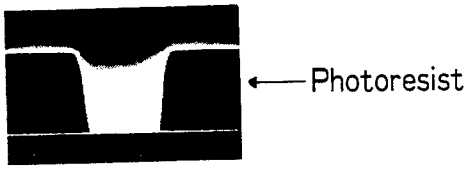


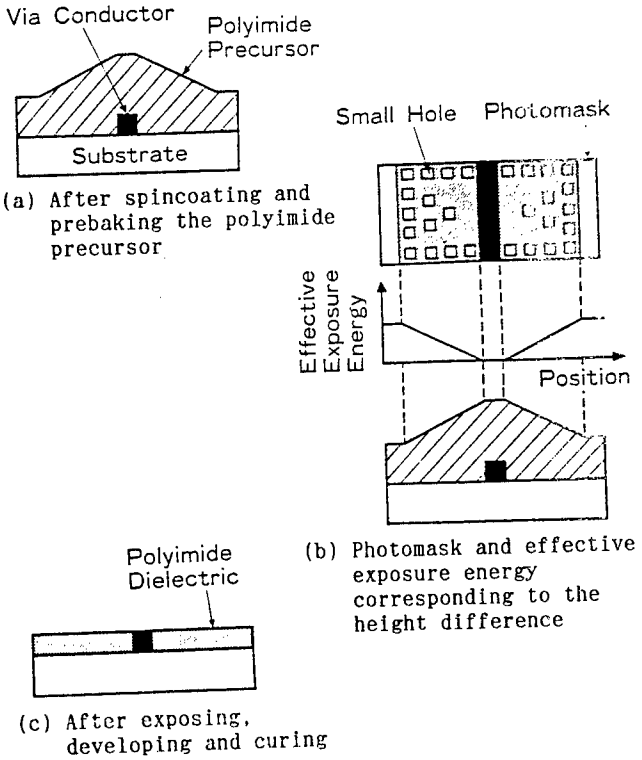
Figure 2 Good-shaped pattern cross-sections of positive photoresist

Figure 3 Cross-section of copper conductor

(2) Dielectric Layer Formation

A polyimide dielectric layer must be planarized to stack an upper via on a lower via in the multilayer substrate.

Figure 4 shows the principle of the novel process for forming a flat polyimide dielectric layer formation by photolithography. After spincoating and prebaking the photosensitive polyimide precursor, there is a height difference between the dielectric layers on the conductor surface and on the substrate because the solvent of the polyimide precursor evaporates (Figure 4(a)). A photosensitive polyimide precursor behaves as a negative photoresist. Because the exposure energy determines the polyimide precursor's solubility in the developer, the exposure energy was controlled by changing the pattern on the photomask according to the height difference to be reduced. The photomask has three sections with different transparencies to the exposure energy (Figure 4(b)): One is transparent for complete polyimide layer formation, one is not transparent for removing the polyimide precursor, and the other has variable transparency continuously controllable by changing the intervals between neighboring small holes. After the polyimide precursor is exposed using this photomask, it is developed and cured to give a flat polyimide dielectric layer (Figure 4(c)).



(a) After spincoating and prebaking the polyimide precursor

(b) Photomask and effective exposure energy corresponding to the height difference

(c) After exposing, developing and curing

Figure 4 Principle of polyimide dielectric layer formation

Figure 5 shows the results of the cross-sectional analysis of the polyimide dielectric layer near the via conductor. When the photomask has only exposure and non-exposure sections, the projection is more than 10 μm, which is about half as thick as the polyimide layer. On the other hand, when the photomask has 0.5 μm-diameter small holes in addition to exposure and non-exposure sections, the projection is small and within 3 μm. These results show that a photomask with small holes corresponding to the height difference to be reduced is effective in reducing the height difference and flattening the polyimide dielectric layer.

(3) Pillar-Shaped Via Formation

Based on the results of these investigations, a via of 3-layer interconnect structure shown in Figure 6. The via conductor is 30 μm square and 25 μm thick per layer. New techniques proposed here can realize a fine and good-shaped via structure with a pillar-shaped conductor and a flat polyimide dielectric layer.

Figure 7 shows measurements of via electrical resistances using the substrate shown in Figure 8. The cross-sectional diameter of the via ranged from 30 μm to 130 μm. A conventional via has an electrical resistance per via of about 0.8 mΩ when the via diameter, d, is about 100 μm. A new pillar-shaped via of the same has an electrical resistance that is less than 0.5 mΩ is proportional to d^{-2}. Thus, the electrical resistance of a pillar-shaped via conductor is about 30 % less than that of the conventional one.

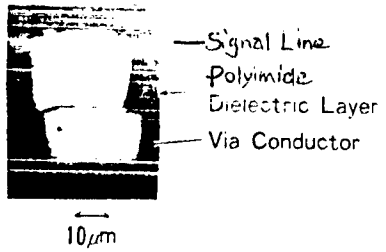


Figure 6 Cross-section of 3-layer interconnect structure

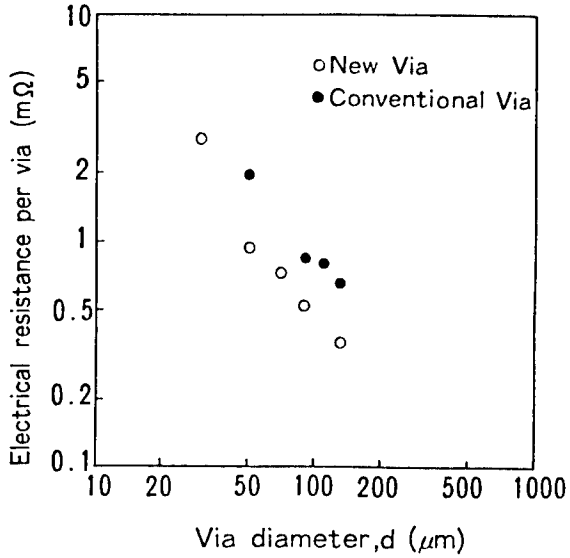


Figure 7 Measurements of via electrical resistance

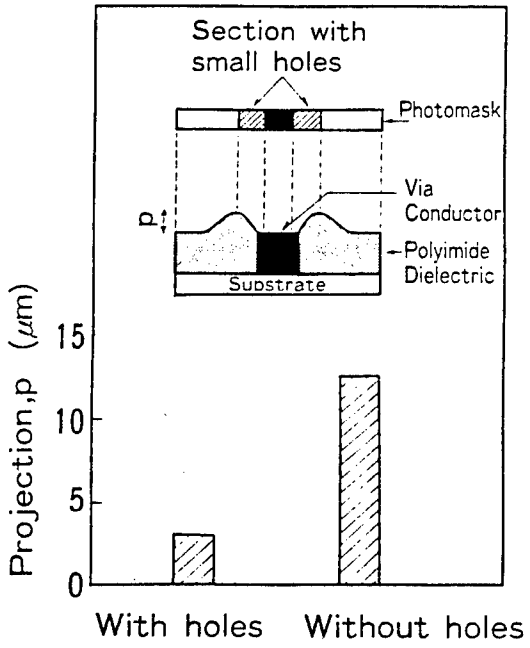


Figure 5 Projection of polyimide dielectric layer

Figure 8 Substrate for measurements

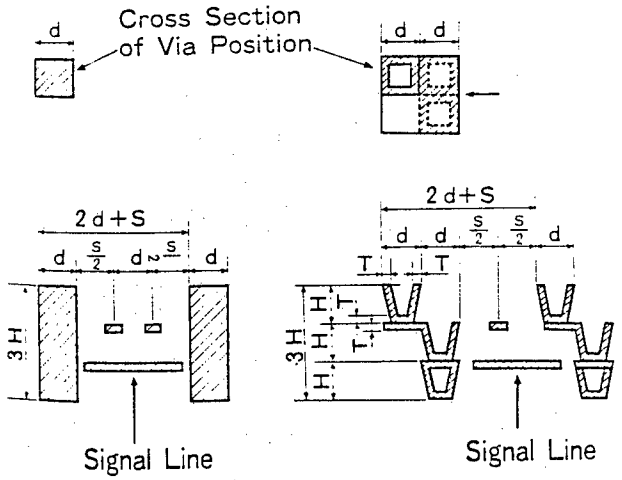
Discussion

Let us consider the area required to interconnect several layers and the thermal conductivity in a multilayer substrate with new vias.

Figure 9 shows the structure of a 4-layer substrate and connections including the vias. Here the via diameter, d, is 50 μm, via thickness, H, is 25 μm, and the upper via pitch, 2d+s, is 200 μm. In the conventional via shown in Figure 9(b), the upper via cannot be stacked on the lower one, so the structure is spiral and the area occupied by the via, $4d^2$, is at least 10,000 μm^2. The interval between neighboring vias, s, is 100 μm, and there is one signal line in the center position. On the other hand, in the new via shown in Figure 9(a), the area, d^2, is 2,500 μm^2, the interval between neighboring vias, d+s, is 150 μm and there is room for at least two signal lines between two vias.

The characteristics of the via were evaluated by estimating the density of interconnection signal lines and the thermal resistance as shown in TABLE I. Comparing the unit areas shown in Figure 9, the density of interconnection signal lines is twice as large in the new via as in the conventional one. When the via is only to radiate heat, the thermal resistance is 76 K/W for the new via and 163 K/W for the conventional one. Thus, the thermal resistance of the new via is less than 50 % that of the conventional one.

These results show that a pillar-shaped via structure fabricated by this new process is suitable for high-performance and high-power electronic systems.



(a) New via (b) Conventional via

Figure 9 Models of 4-layer interconnection structure

TABLE I Characteristics of the via conductors

	New Via	Conventional Via
Density of the Interconnection Signal Lines (per unit area)	2	1
Thermal resistance (K/W)	76	163

Conclusion

A new pillar-shaped via structure has been developed for a Cu-polyimide multilayer substrate. A fine rectangular via pattern is formed by electroplating using a thick positive photoresist, and a flat polyimide dielectric layer is formed by photolithography. An experimental Cu-polyimide 3-layer interconnect substrate with a pillar-shaped via structure had a via diameter ranging from 30 μm to 130 μm with a thickness per layer of 25 μm. Furthermore, a 4-layer interconnect substrate had twice the density of the interconnection signal lines and less than 40 % of the thermal resistance of a conventional one. This pillar-shaped via structure is suitable for high-performance electronic systems which enable high-speed signal transmission.

Acknowledgment

The authors would like to thank Takaaki Ohsaki, Toyoshi Yasuda, Fuminori Ishizuka and Toshifumi Suzuki for their technical advice.

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A TECHNOLOGY FOR HIGH DENSITY MOUNTING UTILIZING POLYMERIC MULTILAYER SUBSTRATE

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ABSTRACT

Nowadays multilayer substrate with excellent characteristics have been required increasingly for miniaturizing, and achieving high level functions. The authors have attempted to produce a high density functional module including new polymeric substrate technology. The module consists of three parts: the multilayer substrate, the block including electrical parts and the thin film resistor sheet. A polycarbonate resin film was selected as the substrate. A conductive paste made from silver powder and thermoplastic resin binder was printed on the polycarbonate resin film. Then these films are piled up and laminated by thermal press. The parts are placed and molded into a shape of block with UV curing resin. The resistor layer is formed by sputtering a thin NiCr film on the polyimide resin coated stainless steel plate. The parts block and the resistor sheet are aligned to the substrate corresponding to their electrodes, then adhered each other with adhesive resin. In this paper, we discuss the actual processes of the manufacturing of the module according to the new mounting method.

crystal display pocket TV, the handy size personal computer, the pocket bell, the video movie camera and the electronic still camera, the requirements for electronic systems miniaturization are still strong. Accordingly, tecnology is still needed for mounting parts in higher density. The anthors have been trying to develop a new high-density mounting technology, which is based on the plastic multilayer structure, aiming at a microminiaturized mounting method and a simpler process. This report describes the process for developing the functional block module, trially fabricated using plastic multilayer substrate fabrication method and the new mounting method, using the film resistor element.

2. FUNDAMENTAL TECHNOLOGY IN NEW MOUNTING METHOD (1)

2.1 Plastic Multilayer Method

This procedure makes the manufacturing possible for the multilayer substrate without any special processes by thermally pressing the plurally laminated films of thermoplastic resin , which has previously been perforated and is printed with the conductor paste, whose binder is thermoplastic resin. The fabricating processes and structure for the plastic multilayer substrate are shown in Fig.1. Features in this plastic multilayer substrate technology are the capability of easily fabricating the multilayer substrate through the simple process without any special restricton in regard to the number of conductor layers, the ability to make one layer remarkably thin, since the thermoplastic film is used as one layer, and the fact that the fabricated plastic multilayer substrate is provided with flexibility, thermal shock resistance and bendability, whose levels are higher than those for the conventional printed circuit board.

1. INTRODUCTION

The commercial state of the hybrid IC, fabricated by the thick film technology, are adoption of Cu paste and multilayer substrate. Aiming at higher desnity, higher layer multiplication and higher function multiplication, the technology for green sheet multilayer wiring substrate, Cu multilayer wiring substrate, low temperature concurrently fired substrate, high heat conductive substrate and film-condenser element have positively been researched and developed. On the contrary, for the printed wiring board made of resin, technology regarding single and double sided boards, and multilayer board has already been established. Although the techonlogy for fine wiring pattern with multilayer board and for mounting with SMD have been developed to a certain degree, research and development for improving the board by adopting the new manufacturing process for the board and the introduction of a film element can not be said to have been sufficiently promoted. On the other hand, viewed from the product side, though miniaturization, high level functions and multi-functions have been realized in the liquid

(2)

2.2 Film Resistor Array Sheet

The chip type resistor is conventionally used as the resistor on the printed circuit board. However, if resistor can be taken the form of a film resistors array, it becomes possible to provide it as a part of the substrate resulting in reducing the space required for the parts, the reduction in the required quantity of parts and the reduction in complicated processes involved in mounting. This means the module reliability can be expected to be improved. The technology has been developed for arranging the metal thin film resistor elements, which have resistance characteristics equivalent to those for the chip type resistor suitable to this

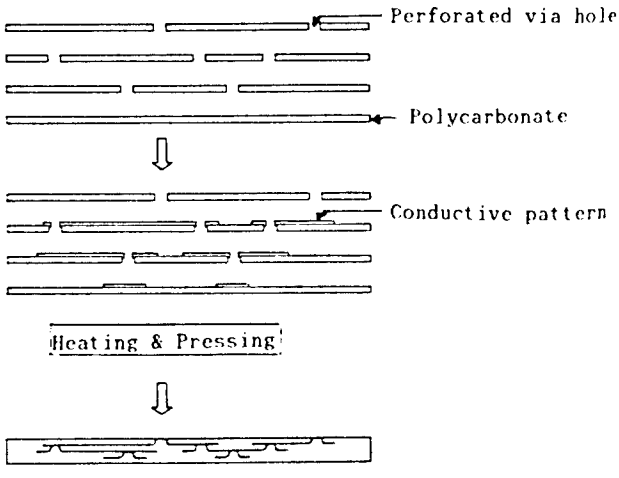


Fig.1 New polymeric multilayer substrate technology constructing processes

purpose, to gather on the sheet in the arrayed state. By applying this technology to the above mentioned plastic multilayer substrate, a substrate provided with the desired resistance resistors can be realized. The sheet structure for the metal thin film resistor element, developed for this purpose, is shown in Fig. 2. Fundamental characteristics of this resistor are shown in Tab.1.

(3)

2.3 Level Connection Technology

For the mounting method aimed at in this report, since the substrate level and the film resistor sheet level are required to be connected with each other's level, connection cannot be made using solder. Accordingly, research and development on the level connection method has become necessary. For this reason, this process, the technology for connecting substrate levels to each other has been established. As shown in Fig.3, level connectoin is accomplished to be made by thermal press, applying an adhesive agent after the plastic multilayer substrate and film resistor sheet are appropriately aligned. At this time, by having the conductor printed on either plastic multilayer substrate side or resistor sheet side referring to the portion to be connected, satisfactory connection can be made. By this method, a highly stable connection can be obtained. Since this method is applicable to level connection with each other, this is also applicable to connecting the parts block, described later, with this substrate.

3. FUNCTIONAL BLOCK MODULE DESIGN BASED ON NEW MOUNTING METHOD

3-1 Fundamental Structure

The following reports on the functional block module trially fabricated according to the new

testing item	test sample			JIS6407 specified value	test condition
	50Ω	2kΩ	50k Ω		
resistance tolerance	±5%	±5%	±5%	J (±5%)	
high frequncy charactristics	Rf/Rdc 1.00	0.99	0.87		at 100kHz
current noise	-26.4db	-20.9db	-21.3db		
thermal coef-ficient ratio	<100ppm	<150ppm	<150ppm	<50kΩ <300ppm >50kΩ <500ppm	
high humidity storage test	<1%	<1%	<1%	<5%	70 ℃ 90-95% 500H
high temprature storage test	<1%	<1%	<1%	<3%	80 ℃ 500H

※ Though high humidity and high temperature tests were made under loading, according to JIS6407, in this case these tests were carried out unloading.

Tab.1 NiCr thin film resistor characteristics

mounting method through applying the fundamental technology described in item 2. The fundamental concept is as shown in Fig.4. First, the plastic multilayer substrate, the parts block and the thin film resistors sheet are individually prepared. Second, as shown in Fig.4(b). the plastic multilayer substrate, the parts block and the thin film resistor sheet are aligned, thermally pressed and connected after applying the adhesive agent. Third, as shown in Fig.4(c), the board is bent and the functional block, structured three dimensionally by the three parts layers structure and the two substrate layers structure, is fabricated. In the following, the actual trial fabrication processes for this functional block module, based on the fundamental concept, is described in detail. The circuit used as the motif is a kind of liquid crystal drive circuit, which is shown in Fig.5.

3.2. Parts Layout

Prior to making a wiring design for the substrate, since the high multilayer structure, which is the feature of the plastic multilayer substrate, is easily accomplished and the board wiring flexibility is high, making good use of this feature, the processes are carried out as follows. First, the parts layout is determined and two kinds of parts blocks, A and B, are prepared. On A block, relatively large parts, such as the ICs, the high capacity condensers and the large chip type resistors at a rated power are laid together. On B block, relatively small and standard parts, such as the transistors and diodes are laid out. The parts layout drawing, based on this design concept, is shown in Fig.6. The distance between the parts is determined as to make the smallest mounting space considering the allowance on the processes.

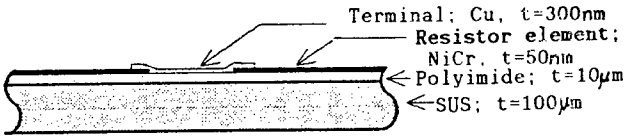


Fig.2 Metal thin film resistor array sheet cross sectional view

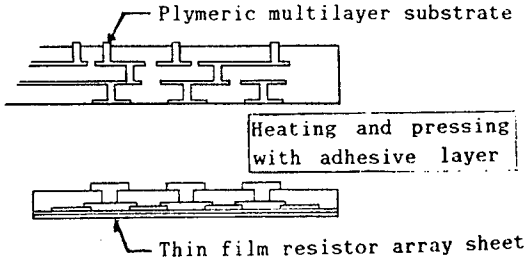


Fig.3 Lamination between polymeric multilayer substrate and resistor array sheet

3.3 Pattern Design

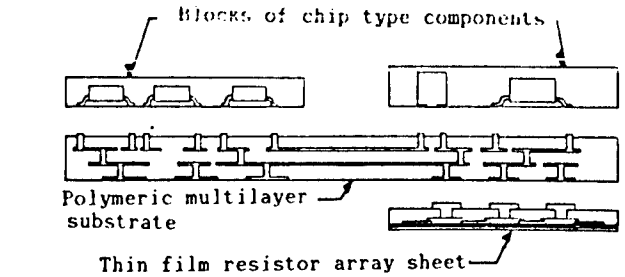
The following design standards are applied to the pattern design.

Conductor width/space width	0.2mm/0.2mm
Through hole diameter	0.2mmϕ
Land diameter of through hole portion	0.4mmϕ
Minmum through hole pitch	0.5mm

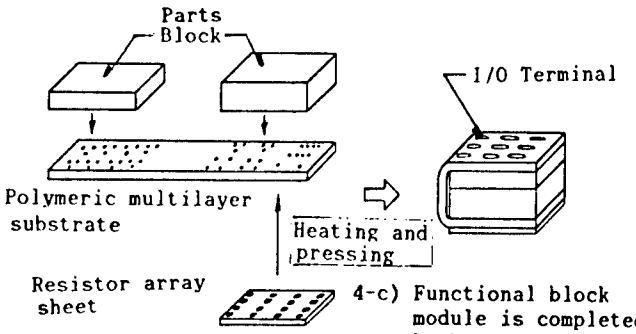
A layout drawing for wiring design, suitable for the parts layout described above is shown in Fig.7. It is made by applying the CAD technique with these design rules. This circuit patterns are accomplished by wiring design for the five conductor layers.

3.4 Thin Film Resistor Pattern Design

The resistor pattern is designed to allow the normal YAG laser trimmer to be used for the thick film resistor, and also it is designed to make the widest possible resistance adjustment range. The thin film resistors sheet is designed to have five lines of unit resistor cells laterally and five lines longitudinally, for 25 pieces resistors total within 13.5mm by 15mm sheet. Fig.8 shows one resistor cell pattern. In this pattern, the possible resistance adjustment range is from 100 ohms to 100 kilo-ohms by the trimming operation for separating the resistor pattern. As the two pieces of low resistance, the chip type resistors are applied in the trial manufacturing at this time.



4-a) Individual components are previously manufactured.



4-c) Functional block module is completed by bending substrate

4-b) Individual components are laminated at the same time

Fig.4 Basic construction model functional block module

4. TRIAL FABRICATION OF FUNCTIONAL BLOCK BY NEW MODULE MOUNTING METHOD

4.1.Parts Block Fabrication

The parts blocks are fabricated according to the processes shown in Fig.9. All the parts selected from the SMD parts are mounted on specified position on the adhesive sheet. The UV curing resin is injected. The adhesive sheet is split off, after the resin is cured, to obtain a parts block for a flat level, on whose surface all the terminals of parts are exposed and aligned.

4.2. Plastic Multilayer Substrate Fabrication

As the thermoplastic resin, 50 μm thick polycarbonate resin film is adopted. For the first step, this film is perforated according to the instruction from the design data by CAD. The numerically controlled drilling machine is used for drilling to make the holes of 0.2mmϕ. Through holes in four different patterns (refer to Fig.10) are perforated in a film sheet. Screen printing is carried out on film including the four conductor layers at one time. The screen printing is accomplished using the factory-made silver system thick film conductor paste, for which binder thermoplastic resin is used. The conditions for printing are as follow.

[illegible]n	325mesh stainless screen
Emulsion thickness	10μm
Printer	auto screen printer with pattern recognizing equipment

4.3 Connecting Parts Block and Film Resistor Sheet with Plastic Multilayer Board

The electrode for connection is made by printing only the connection portion of the substrate side with conductive paste. The adhesive agent in the liquid epoxy resin system is coated on the parts

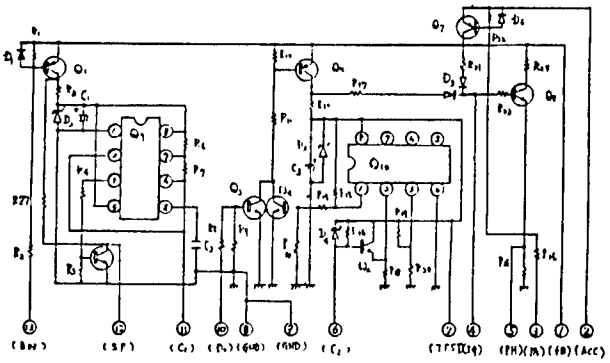


Fig.5 Trial product circuit

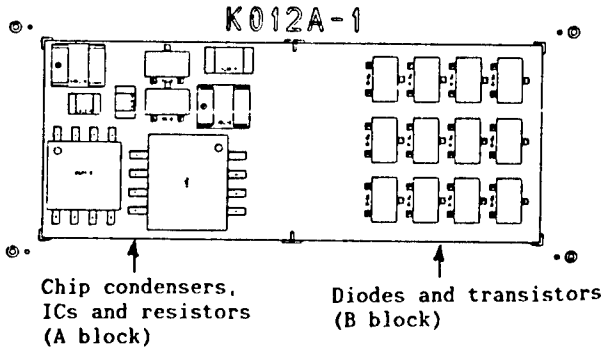


Fig.6 Parts arrangement

block and the film resistors sheet. After applying about 5kg/cm² pressure, the resin is cured at 100°C. The substrate is bent as shown in Fig.4(c) above. It is connected by epoxy resin adhesive agent in the same way as described above. The functional block module thus fabricated is shown in Photo.1.

5. TRIAL FABRICATION RESULTS AND PROBLEMS

Photo.2 shows the hybrid circuit module whose base is an alumina board and its module is producting in present time. This is the same kinds of circuit as that the authors trially fabricated in this time. The results obtained, after comparing two modules, are shown in Table 2. In the new circuit module, the projected area, the volume and the weight are markedly reduced. The features of this mounting method are arranged as shown in the following.

1) The plastic multilayer substrate, when compared with a conventional hybrid IC, is thinner and bendable. Accordingly, the three dimensional board structure, the multi-structure of parts layers, and the high density mounting in the minimum space become possible.

2)Since the film resistor elements are able to be accomodated in the form of the film array, the quantity of parts can be markedly reduced. Also it can be made thinner.

3)Since the fabricated functional block module has only the I/O terminals exposed outside and has other elements and conductor sealed with the high insulative thermoplastic resin, its ability to resist environmental condition is high and its handling becomes easy.

4)Since the outward form is regular size, the increasing the function is easily realized through piling up on the other functional block module.

5)This mounting process is suitable for mass production.

However, this new mounting method is not yet a completed method. In future, we must establish the confirmation of reliablity and the conditions of practical mass production processes of the modules.

6. CONCLUSION

A new mounting method is proposed for fabricating a functional block module by level connecting the plastic multilayer substrate using the thermoplastic resin film, with the parts block and the thin film resistors sheet. A markedly more compact mounting method, as compared with the conventinal mounting method was proved to be feasible by trially fabricating an actual circuit.

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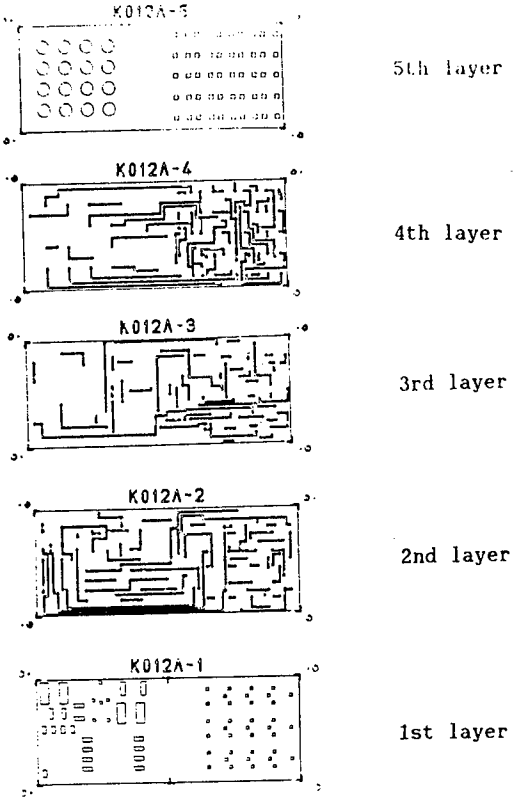
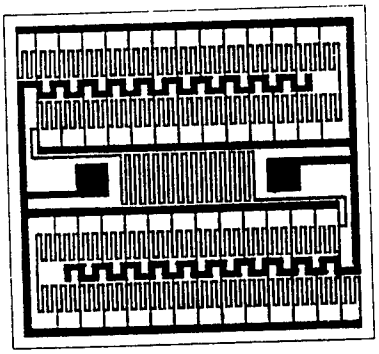
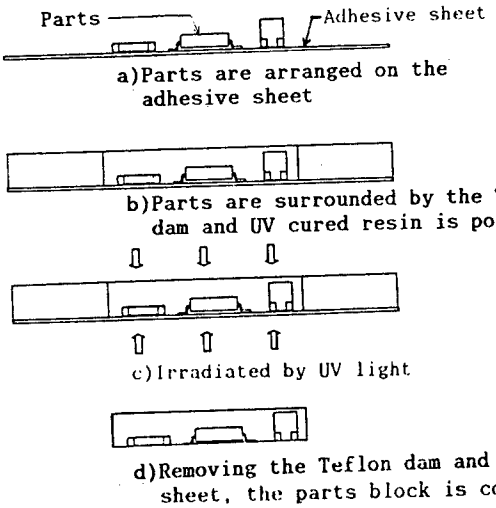


Fig.7 CAD lavout conductor pattern for polymeric multilayer substrate



Max.line width; 60μm
Min.line width; 10μm

Fig.8 Unit resistor cell



a)Parts are arranged on the adhesive sheet

b)Parts are surrounded by the Teflon dam and UV cured resin is poured

c)Irradiated by UV light

d)Removing the Teflon dam and the adhesive sheet, the parts block is completed.

Fig.9 Parts block manufacturing process

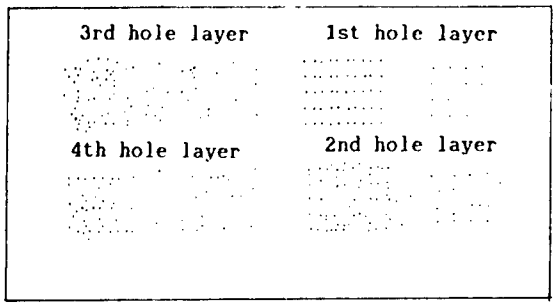


Fig.10 Layout of through holes

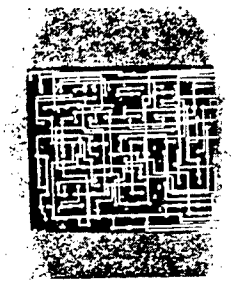


Photo.1 New functional block module

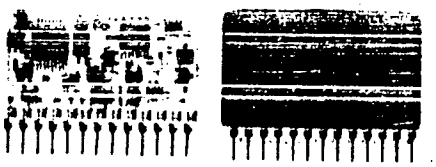


Photo.2 Conventional alumina hybrid module

Tab.2 Comparison between functional block module and conventional alumina hybrid module

	new functional block module	alumina hybrid module
number of conductive layers	5	2
side of conductive pattern formation	double	single
projection area ratio	0.27	1
volume ratio	0.27	1
weigt ratio	0.35	1

Cu INTERNAL ELECTRODE MULTILAYER CERAMIC CAPACITOR

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ABSTRACT

We have developed a new process for the manufacture of multilayer ceramic capacitor with copper internal electrodes (CuMLC). The present method employs low firing $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$ and copper oxide paste as dielectric and conductive materials, respectively. In this fabrication method, the organic binder is burned-out in air, followed by reduction of copper oxide and sintering. The following electrical properties of CuMLC were obtained: Dielectric constant, 11000, dissipation factor at 1KHz, 1Vrms, 0.5%, insulation resistance, >10000ΩF (at 25°C). In the load humidity test (85°C, 85%RH, 50V), no degradation of insulation resistance was found during 1000 hours of testing.

INTRODUCTION

Recent advancements in IC and LSI technologies have contributed to rapid progress in the development of smaller, higher packing density and higher frequency electronic devices. To keep up with this trend, compactness, high reliability, and low cost chip construction are also being demanded of passive components that form electronic circuits. Among many chip components, the number of multilayer ceramic capacitors (MLC) produced is increasing rapidly due to their following advantages: (1) No polarity, small size and large capacitance per volume, (2) High moisture resistance and high reliability, (3) Small internal inductance and excellent characteristics at high frequency. Conventional MLCs use noble metals such as palladium and platinum as their electrode material because of their favorable properties, i.e. these noble metals have high melting points and are hardly oxidized, so that they can serve as electrodes when the noble metals and dielectric ceramics in layers are fired simultaneously in air. However, these noble metals are expensive. In addition, to produce MLC with large capacitance to replace conventional aluminum or tantalum electrolytic capacitors, the number of layers must be increased and thus a large amount of electrode materials is required. The high cost of the electrode materials has resulted in substantial increase in the manufacturing cost of MLC. In other words, reduction of the electrode material cost is the most important key to reduce the manufacturing cost of large capacitance MLC for commercial use. In order to reduce electrode material cost, the industry has been studying the use of less expensive Ag-Pd alloy[1] or base metals[2] such as Fe, Co, Ni and Cu in place of more expensive Pd and Pt.

Copper is one of the most promising candidates for internal electrode material due to its low cost, high conductivity and reliability. However, copper, easily oxidized if fired in air, requires a neutral or reducing atmosphere during firing. Meanwhile, if fired in a low oxygen partial pressure atmosphere, many dielectric materials become semiconductive, with insufficient insulation resistance to serve as capacitor materials.

The green sheet technique has been used in manufacturing MLC. Green sheet contains a large amount of organic binders. Therefore, when firing takes place in a low oxygen atmosphere, the most important and difficult problem is to remove these organic binders. The carbonaceous residues prevent consolidation of the dielectric ceramic material into a dense ceramic body. As a result, the insulation resistance of the dielectric layer decreases.

Accordingly, realization of MLC with copper internal electrodes requires a low firing dielectric material that provides high insulation resistance if fired in a low oxygen partial pressure atmosphere, and a firing process that can completely remove the organic binders in the dielectric green sheet. We have solved these technical problems and successfully developed multilayer ceramic capacitor with copper internal electrodes.

In this report, a detailed description is given of a new copper metallizing method we have developed and also of a dielectric material which makes our engineering method feasible.

MATERIALS

(1) Dielectric material

High purity reagents of PbO, MgO, Nb_2O_5 and CuO were used as starting materials. We employed a conventional material preparation method but used the technique invented by Swartz et al.[3] to facilitate the formation of a pyrochlore-free perovskite phase. Mixture of MgO and Nb_2O_5 was calcined at 1000°C for 6 hours. Prefabricated $MgNb_2O_6$ was mixed with appropriate amounts of PbO and CuO. The mixture was then calcined at 800°C for 2 hours. Calcinations were carried out in air. The calcined dielectric material was milled and it was confirmed that pyrochlore phase was not generated by X-ray powder diffraction using CuKα radiation.

(2) Conductive material

High purity reagent of CuO was calcined at 800°C in air for 2 hours and milled into powder with about 3 um average particle size. Particle size was measured by a centrifugal automatic particle analyzer. The CuO powder and vehicle, organic binder ethylcellulose dissolved in terpineol solvent, were dispersed using a roll mill to make conductive paste.

PROPERTY EVALUATION METHOD

The dielectric material, with the addition of 5wt% PVA binder, was pressed into a disk (10mm in diameter, 2-3mm thick) under pressure of 1000kg/cm^2. After binder removal by slow heating at 600°C in air, sintering was performed at temperatures between 800°C and 1000°C in nitrogen atmosphere. Heating rate was 300°C/hr and soaking time was 1 hour. To prevent volatilization of PbO, the samples were covered with $Pb(Mg_{1/3}Nb_{2/3})O_3$ powder and stacked inside a sealed MgO vessel when fired. The bulk densities of sintered samples were measured by liquid displacement method using water as the medium. The sintered disk was ground to a thickness of 2mm and In-Ga alloy electrode was applied to measure the electrical properties of the dielectric material. Dielectric constant and dissipation factor were measured using a LCR meter (HP-4274A) at 1KHz with 1Vrms. Insulation resistance was measured using a high resistance meter (HP-4329A), 1 minute after applying 50VDC.

MANUFACTURING PROCESS

Figure 1 shows the process of manufacturing MLC with copper internal electrodes. Multilayered green chip was fabricated by the conventional method from dielectric green sheets and copper oxide paste. The green chip was made into MLC through the processes of burning out binder in air, reduction of copper oxide in hydrogen atmosphere and sintering in nitrogen atmosphere. Figure 2 shows the concept of firing process used for manufacturing CuMLC. Each of the binder burn-out, reduction and sintering process is described in detail below.

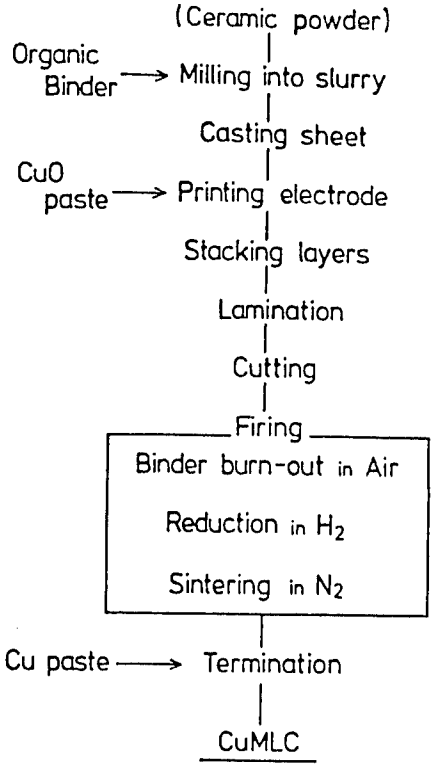

Fig.1 CuMLC manufacturing process

(1) Binder burn-out process

In this process, organic substances, such as plasticizer and binder, contained in dielectric green sheet and conductive paste are removed by heat treatment in air. Copper oxide (CuO) does not change chemically and causes no change in volume, but thermal decomposition of organic binder also occurs. Complete thermal decomposition and removal of organic binder can be achieved because organic binder reacts with the oxygen in air. Binder burn-out temperature was determined by conducting thermal analysis in advance.

(2) Reduction process

In this process, copper oxide is reduced to copper by heat treatment in hydrogen atmosphere. The reductive reaction of CuO to Cu would proceed at a remarkable rate in hydrogen atmosphere at a low temperature. Reduction temperature should be selected so that the dielectric material is not reduced. During the reduction process from CuO to Cu, volume changes, but since some adhesion between the conductive layer and the dielectric layer was obtained in the binder burn-out process, neither delamination of the conductor layer nor cracking of the dielectric layer occurs.

(3) Sintering process

In this process, the densification of dielectric ceramic body is achieved. Sintering is carried out in nitrogen atmosphere in which copper electrode is not re-oxidized. A commercial continuous belt furnace is employed. Since organic binder is completely removed, no delicate atmospheric control is required and a densely sintered ceramic body can be given in this process.

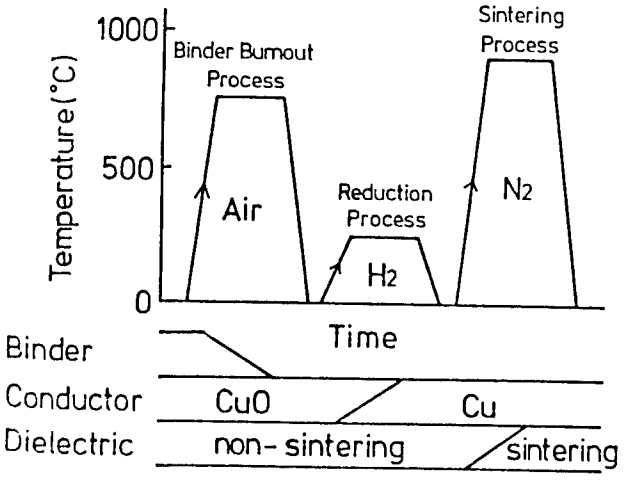

Fig.2 Temperature and atmospheric profiles of the firing process

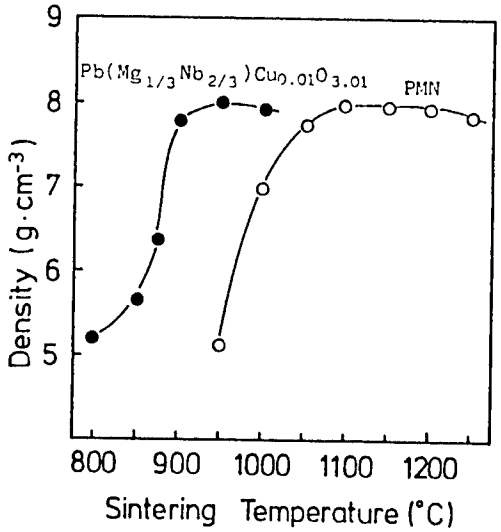

Fig.3 Variation of density with sintering temperature for $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$ and PMN

PROPERTIES OF DIELECTRIC MATERIAL

For the present technique, the dielectric material is required to have the following properties: (1) The dielectric material must be sintered densely at a temperature lower than the copper melting point (1083°C). (2) The dielectric material should provide high reduction resistance and should experience no drop in insulation resistance if fired in a low oxygen content atmosphere in which copper is not oxidized.

We added CuO to $Pb(Mg_{1/3}Nb_{2/3})O_3$ (PMN), making it possible to sinter PMN at a low temperature. Figure 3 shows the changes in density of $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$ as a function of the sintering temperature. The data for PMN are also shown in the figure. As shown, rapid densification occurs above 850°C and reaches a maximum value at 950°C for $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$ whereas PMN is sintered above 1100°C. Figure 4 shows scanning electron micrographs of the fracture surface of $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$ and PMN, both sintered at 950°C. As is evident from the two SEM photographs, addition of CuO to PMN causes rapid grain growth at 950°C. Figure 5 shows the temperature dependence of the dielectric constant and the dissipation factor of $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$. A Curie temperature is around -5°C. At 25°C, the dielectric constant is 11000 and the dissipation factor is 0.5%. The insulation resistance is $2.9 \times 10^{12}\Omega$cm, and $2.3 \times 10^{12}\Omega$cm at 25°C and 85°C, respectively. The temperature dependence of the dielectric constant meets Z5U specification of the EIA standard.

STUDY OF PROCESSING CONDITIONS

(1) Binder burn-out process

Figure 6 shows the effects of binder burn-out temperature on properties of CuMLC. Binder burn-out temperature was maintained for two hours. The chip capacitors were fabricated through binder burn-out, reduction of CuO at 200°C for 5 hours and sintering at 950°C for 1 hour. As is clear from this figure, the capacitors do not provide satisfactory properties if binder burn-out temperature is too low or too high. Specifically, at an excessively low burn-out temperature, some binder will remain in the dielectric green sheet. This residual carbon hampers the progress of the dielectric material sintering, resulting in poor capacitor properties. At an excessively high burn-out temperature, on the other hand, the dielectric material will be sintered excessively such that CuO is hardly reduced to Cu in the following reduction process. CuO remained in the electrodes cannot serve as electrode after sintering, thus the effective area of the electrodes will decrease.

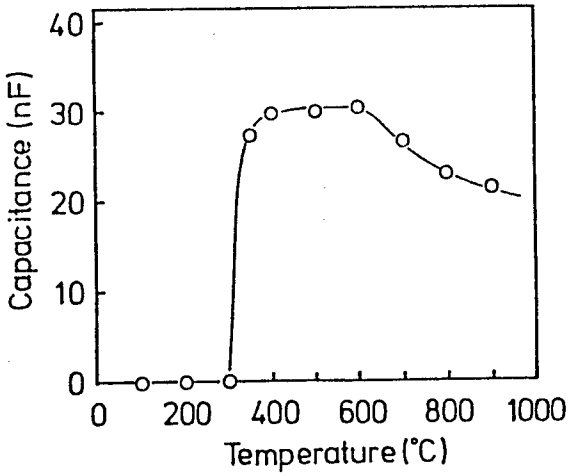

Fig.6 Effect of binder burn-out temperature on capacitance of CuMLC

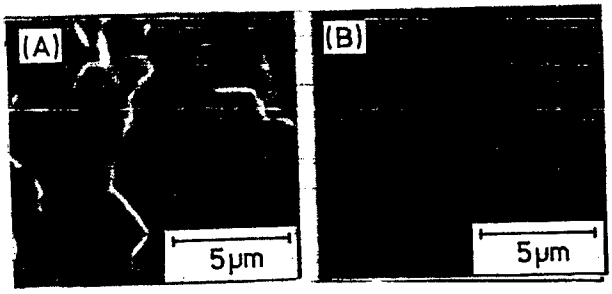

Fig.4 SEM photographs of the fracture surface of (A) $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$ and (B) PMN, both sintered at 950°C

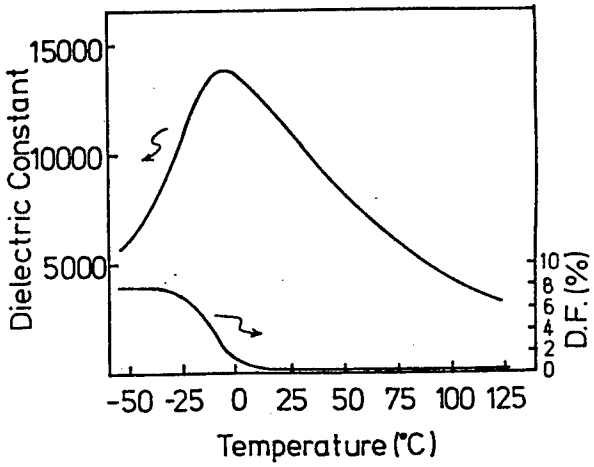

Fig.5 Variation of dielectric constant and dissipation factor with temperature for $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$

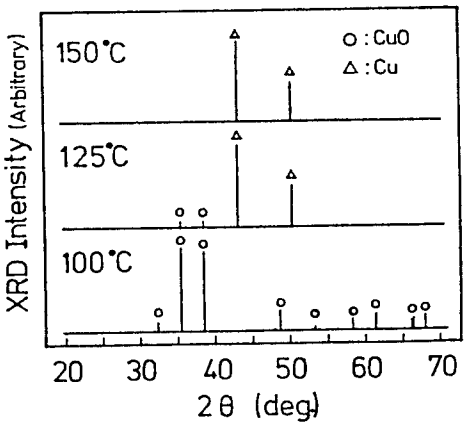

Fig.7 XRD patterns of CuO heat treated at various temperatures in H_2 atmosphere

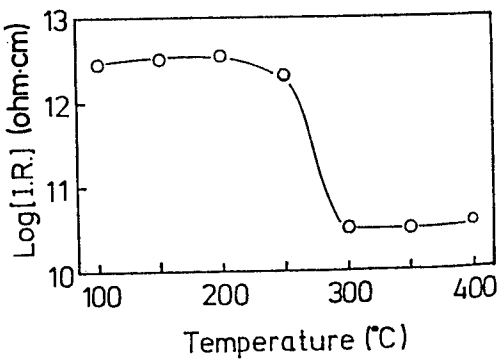

Fig.8 Variation of insulation resistance with reduction temperature for $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$

(2) Reduction process

In this process, it is necessary to reduce CuO to Cu in the electrodes without reducing the dielectric material. Figure 7 shows X-ray diffractograms of copper oxide after reduction. Figure 8 shows the insulation resistance of the dielectric material as a function of the reduction temperature. Copper oxide powder and the dielectric material were heat treated for 5 hours in H_2 atmosphere. The dielectric was fired at 950°C prior to measuring the insulation resistance. As is clear from the figures, with heat treatment at a temperature higher than 150°C. CuO is completely reduced to Cu, and even at 250°C insulation resistance of the dielectric material does not show a significant drop and is maintained at higher than 10^{12} (Ωcm). Thus, according to this reduction process, it is possible to independently reduce CuO to Cu without reducing the dielectric material if the temperature and time for heat treatment in H_2 are at specific values.

CHIP CAPACITOR PROPERTIES

We examined various properties of CuMLC we manufactured by the above-mentioned method. The green sheet we used was 35μm thick. The number of dielectric layers was five. The green chip was fired for burning out binders at 600°C and for reduction at 200°C. Sintering was performed at 950°C for 1 hour. External electrodes (E.I. Du Pont #9153 copper paste) were applied by firing at 900°C. Figure 9 shows a SEM photograph of the fracture surface of CuMLC in which Cu electrode and dielectric layer are 7μm and 25μm thick, respectively. Figure 10 shows the DC bias dependence of capacitance. Data from representative Z5U chip capacitor made from modified $BaTiO_3$ are also shown in the figure. CuMLC fabricated in this study shows superior DC bias dependence compared to the conventional $BaTiO_3$ capacitor. Figure 11 shows the results of the load humidity life test (85°C, 85%RH, 50V bias). Each property shows no deterioration after 1000 hours of testing. As is clear from these results, a completely sealed and gas-tight multilayered structure is given of our CuMLC. Representative properties of the chip capacitor described above are shown on Table 1.

CONCLUSION

Newly developed manufacturing method and material make it possible to produce multilayer ceramic capacitor with copper internal electrodes (CuMLC). A dielectric material of $Pb(Mg_{1/3}Nb_{2/3})Cu_{0.01}O_{3.01}$ can be sintered lower than 1000°C, providing high dielectric constant and high resistivity. The fabrication method requires no delicate atmospheric control in binder burn-out, reduction and sintering process, thus easy process control is accomplished. CuMLC fabricated in this study has excellent electrical properties and reliability. We are convinced that our CuMLC technology can significantly reduce the manufacturing cost of multilayer ceramic capacitors with large capacitance.

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3) S.L. Swartz and T.R. Shrout, "Fabrication of perovskite lead magnesium niobate," Mater. Res. Bull., 17 (1982) 1245-1250.

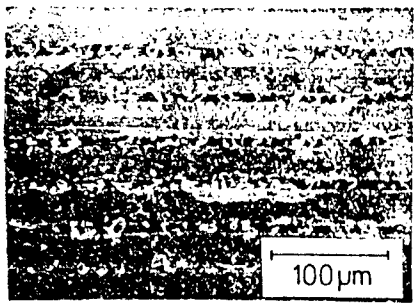

Fig.9 SEM photograph of the fracture surface of CuMLC

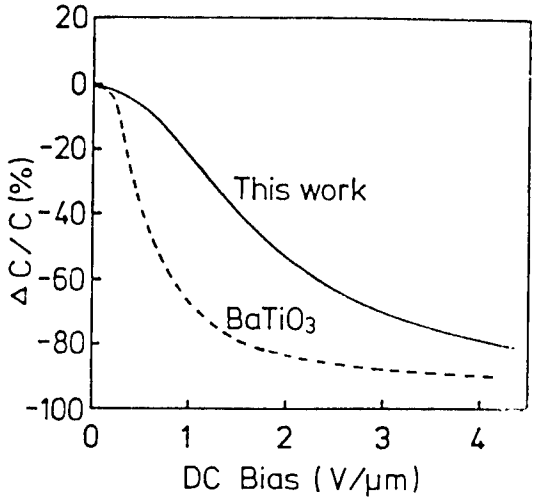

Fig.10 Variation of capacitance with applied DC bias

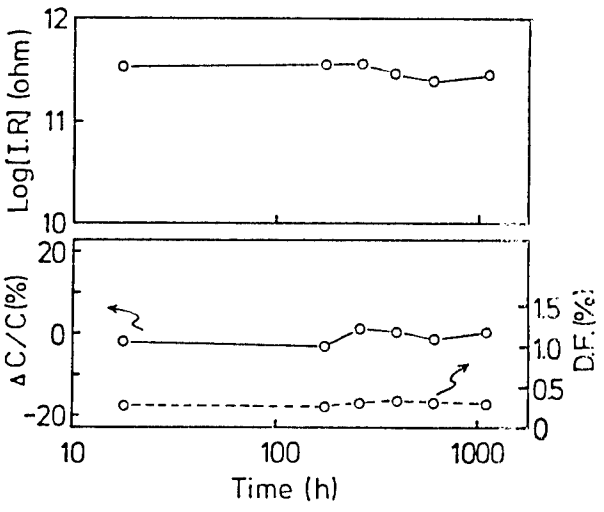

Fig.11 Results of load humidity life test (85°C, 85%RH, 50V) for CuMLC

Table 1 Representative properties of CuMLC

Size (L x W x T)	3.2 x 1.6 x 0.6 mm
Single layer thickness	25 μm
Number of layers	5
Capacitance (25°C)	30 nF
Dissipation factor (25°C)	0.5 %
C·R product (25°C)	10000 ΩF
Variation of capacitance	10°C, +11 % 85°C; -52 %

TANTALUM OXIDE THIN-FILM CAPACITOR SUITABLE FOR BEING INCORPORATED INTO AN INTEGRATED CIRCUIT PACKAGE

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ABSTRACT

As new high speed integrated circuits (IC's) such as gallium arsenide IC (GaAs IC) and emitter coupled logic IC (ECL IC) are coming into use in digital electronic systems, it has become important to employ effective decoupling techniques to insure proper operation of these IC chips. The lengths of package leads and lines should be kept to be minimum or eliminated. One of the most effective ways to reduce switching-noise is to incorporate by-pass capacitors into the IC package. The authors have developed a tantalum oxide (Ta_2O_5) thin-film capacitor which is compatible with die-bonding by gold-silicon (Au-Si) solder and hermetic glass-sealed packaging. Its lower electrode is a metal plate, the upper one is a metal thin film. This report describes a Ta_2O_5 thin-film capacitor which uses a rolled tape of iron-42%nickel (Fe-42%Ni) alloy as the metal plate, and aluminum (Al) as the metal thin film. This capacitor can withstand a temperature of 500℃ for more than ten minutes. Thermal coefficient of capacitance is less than 400ppm/deg. in the range of 25℃ to 150℃. The dependence of capacitance on frequency is very small in the range of 1MHz to 1GHz. The dielectric loss tangent ($\tan\delta$) is less than 0.5% at 1MHz. We compared Ta_2O_5 thin-film capacitor's performance with barium titanate ($BaTiO_3$) base single-layer chip capacitor's by measuring the gain of an amplifier which was composed of an amplifier IC chip and a capacitor in a leadless chip carrier package. Incorporating Ta_2O_5 thin-film capacitors into the IC package was confirmed to be a more effective decoupling technique, particularly at more than 100MHz.

INTRODUCTION

Advance in the digital electronic systems, i.e. super computers and graphic terminals, requires higher speed IC's such as GaAs IC and ECL IC. In the field of telecommunications, fiber optics which enable us to process a large number of data simultaneously, must have a smaller sized high speed IC operating at more than 1Gbps. The higher the clock frequency of an IC chip is, the more necessary effective decoupling techniques are to insure proper operation of an IC. The lengths of package leads and lines should be kept to be minimum or eliminated. One of the most effective ways to reduce switching-noise is to incorporate by-pass capacitors into the IC package.

Recently sintered ceramic capacitors have been used as these by-pass capacitors as shown in Fig.1. But in the sintered ceramic capacitors, the dielectric dispersion occurs usually at the frequencies of 100MHz to 1GHz. The dielectric dispersion decreases the dielectric constant and as a result the performance of decoupling is lessened.

This report concerns a new type of by-pass capacitor which has been developed to meet the demand of high performance decoupling techniques. This capacitor has a Ta_2O_5 thin-film dielectric layer deposited on a metal plate, and has efficient by-pass capacitor characteristics. Furthermore, since it is highly stable against heat, Au-Si solder and hermetic glass-sealing can be used which results in reliable mounting.

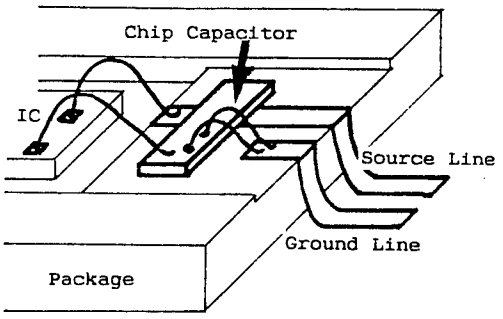


Fig.1. Assembly Of A By-Pass Capacitor In A Package

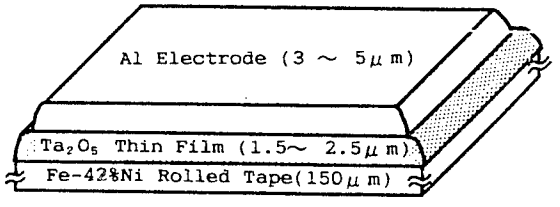
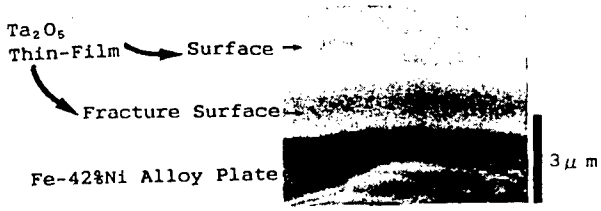


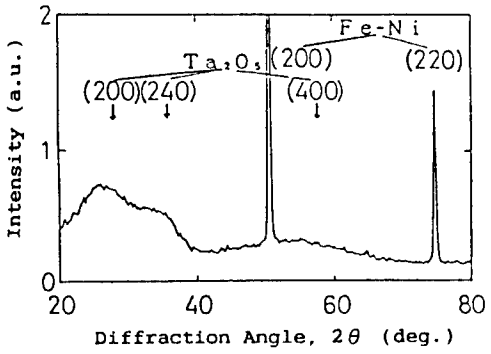
Fig.2 Consruction Of The Ta_2O_5 Thin-Film Capacitor

CONSTRUCTION AND FEATURES

The construction of this capacitor is shown in Fig.2. A Ta_2O_5 thin film is directly deposited on a metal plate. Furthermore, a metal thin film is layerd on the Ta_2O_5 thin film. Its lower electorode is a metal plate; the upper one is a metal thin film. This report describes a Ta_2O_5 thin-film capacitor which uses a rolled tape of Fe-42%Ni alloy as the metal plate, and Al as the metal thin film. Typical thicknesses of these thin films and the metal plate are also shown in Fig.2. Since the thermal expansion coefficient of Fe-42%Ni alloy is closer to that of Ta_2O_5 among various metal plates, the construction is maintained during the heat treatment used in the mounting and packaging processes. Because of very little electric resistance of the Fe-42%Ni metal plate and the Al thin-film electrodes, this capacitor keeps low impedence at high frequencies. The Al thin film adheres well to the Ta_2O_5 thin film and has good wire-bondability. The Ta_2O_5 thin film is not an aggregate of the fine particles, but an extermely flat surface.



(A) SEM Photo. Of The Fracture Surface And Surface



(B) X-Ray Diffraction Pattern

Fig.3 X-Ray Diffraction Pattern And Fracture Surface Of The Ta_2O_5 Thin Film Deposited On The Fe-42%Ni Plate

Furthermore, it is a finely formed thin film without columned structure. Fig.3 shows the X-ray diffraction pattern and the SEM photograph of the fracture surface of the Ta_2O_5 thin film on the Fe-42%Ni alloy plate. The diffraction pattern of the Ta_2O_5 thin film shows unsharply broadened peak of X-ray intensity thus proving that this thin film can be considered amorphous.

The typical characteristics of this thin-film capacitor are summarized in Table 1. Desirable capacitance can be used by varying the area and thickness of the thin film up to 240pF/mm². The unrestricted shape and the total thickness of less than 160μm make it easy to be incorporated into a small package. Since the opposite surface of the metal can be plated with Au, Au-Si soldering can be used when incorporating it into a package.

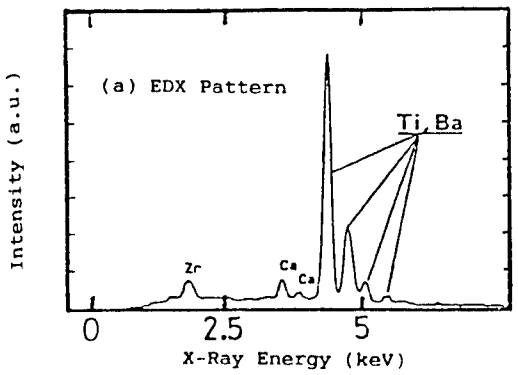
Table.1 Characteristics Of The Ta_2O_5 Thin-Film Capacitor

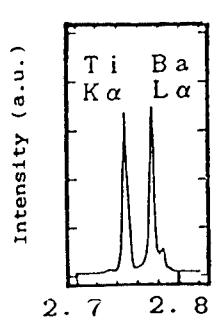
Leakage Current	<1×10⁻⁷A (25℃ ~ 150℃)
Thermal Coefficient	+200~+400ppm/deg. (25℃ ~ 150℃)
Heat Resistance	(500℃ × 5min.) × 8cycles
Capacitance Range	Constant Capacitance Up To 1GHz
Capacitance Density	240 pF/mm² (Max.)
Thickness	< 160μm
Recommended Assmble Method	Wire Bonding (Au Thermo-Sonic) (Al-1%Si Supersonic) Au-Si Soldering Hermetic Glass Sealing

HIGH FREQUENCY CHARACTERISTICS

Measurement Sample

A ceramic capacitor composed of ferroelectrics has been used popularly as a by-pass capacitor. Most of such ceramic capacitors are mainly composed of $BaTiO_3$ or $SrTiO_3$. As mentioned above, ceramic capacitors of ferroelectrics which include $BaTiO_3$ and $SrTiO_3$ have the dielectric dispersion at the frequencies of 100MHz to 1GHz. Fig.4 shows





(b) WDX Pattern

(c) SEM Photo. of Cross Section

Fig.4 Elements And The Cross Section Of The Ceramic Single-Layer Chip Capacitor

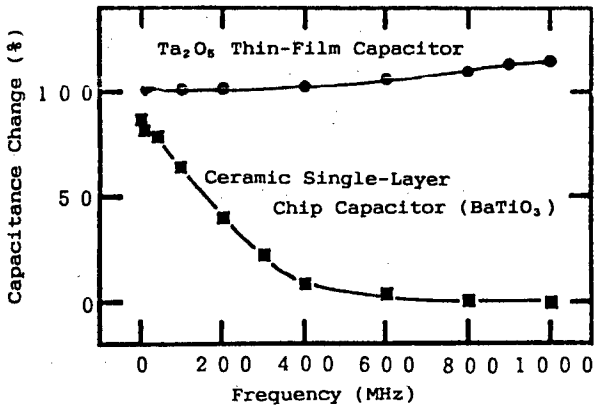


Fig.5 Capacitance Change
Of The Ceramic Sigle-Layer Chip Capacitor
And Ta_2O_5 Thin-Film Capacitor

capacitance of a by-pass capacitor must not change at the high frequencies such as this Ta_2O_5 thin-film capacitor.

EVALUATION OF A BY-PASS CAPACITOR INCORPORATED INTO THE PACKAGE

Measurement

The performance comparison between the Ta_2O_5 thin-film capacitor and the ceramic single-layer capacitor as determined by a by-pass capacitor was estimated, using a wide band amplifier IC packaged in a leadless chip carrier.

the intensity of X-ray dispersive spectrums against the energy and the wavelength, and the SEM photograph of the ceramic single-layer chip capacitor. This chip capacitor is mainly composed of $BaTiO_3$, and has been used at the frequencies higher than 1MHz.

Capacitance change of the Ta_2O_5 thin-film capacitor and this ceramic single-layer chip capacitor were comparatively measured against the frequencies of more than 100MHz.

Measurement of Capacitance Change

The capacitance at the frequencies of a few MHz to 1GHz were measured with an HP4191A impedance analyzer using an HP1609A coaxial test fixture which had very little residual impedance so that the test fixture was not a factor.

The area and the Ta_2O_5 thickness of the thin-film capacitor were $4.5mm^2$ and $2.5\mu m$, respectively. The officially listed capacitance of measured ceramic single-layer chip capacitor was 1500pF.

Results of Measurement

Fig.5 shows the capacitance change of the two kinds of capacitors. The Ta_2O_5 thin-film capacitor maintained nearly constant capacitance for the whole frequency range. But the capacitance of the ceramic single-layer chip capacitor decreased sharply as the frequency increased. At 200MHz the capacitance of the ceramic single-layer capacitor decreased to about 40%, to be negligible at 400MHz. These results prove that this ceramic single-layer capacitor of $BaTiO_3$ has the dielectric dispersion at a few hundreds MHz. For high speed IC's operating at the frequency of more than a few hundreds MHz, the

An example of output spectrum from the amplifier IC is shown in Photo.1. The gain of the amplifier IC was almost constant up to the frequency of about 150MHz at which an oscillating peak was recognized. At the frequency from 150MHz to 300MHz, the gain decreased sharply. The oscillating peak height at about 150MHz should decrease by setting a by-pass capacitor between the source line and the ground line. The higher the capacitance is, the lower the peak height can be expected. Two Ta_2O_5 thin-film capacitors and two ceramic single-layer chip capacitors were used for these measurements.

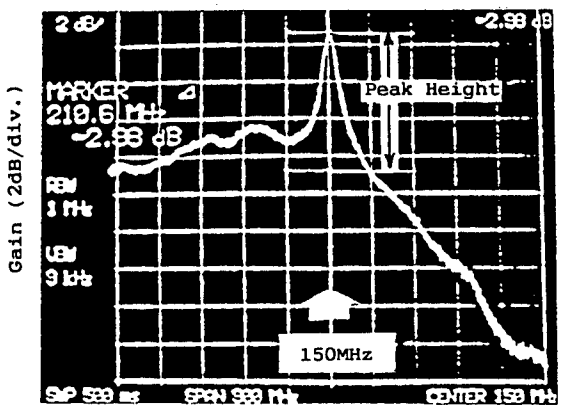


Photo.1 Output Spectrum
And The Oscillating Peak
Of The Wide Band Amp. IC

Fig.6 shows the block-diagram of the test set-up and the photograph of an example of the test samples. The capacitor was incorporated into a wide band amplifier IC's package with Au-Si solder. Sine wave signal was input into the amplifier through an attenuater from a TR4172 spectrum analyzer. The input signal was swept up to 300MHz. The output of the amplifier was connected to the TR4172 spectrum analyzer. A by-pass capacitor was set between the source line of the amplifier IC chip and the ground line.

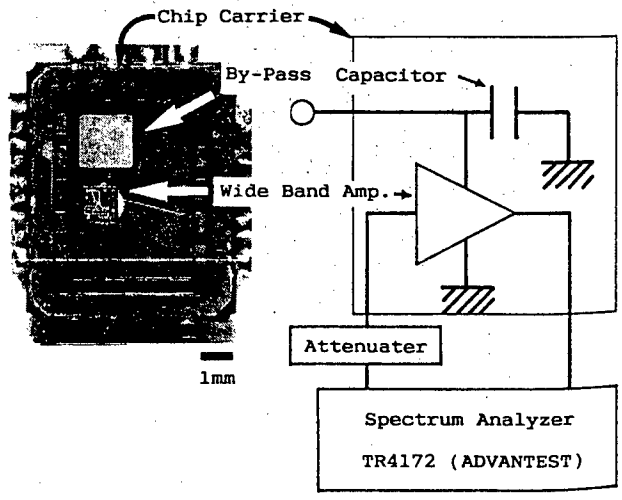


Fig.6 Measurement Set-Up For The Performance
Of By-Pass Capacitors
Incorporated Into The Package

Results and Discussion

The peak heights of each samples were determined by the length of the white pillar in photo.1. The base line of the pillar corresponds to the gain level at the lowest frequency. Fig.7

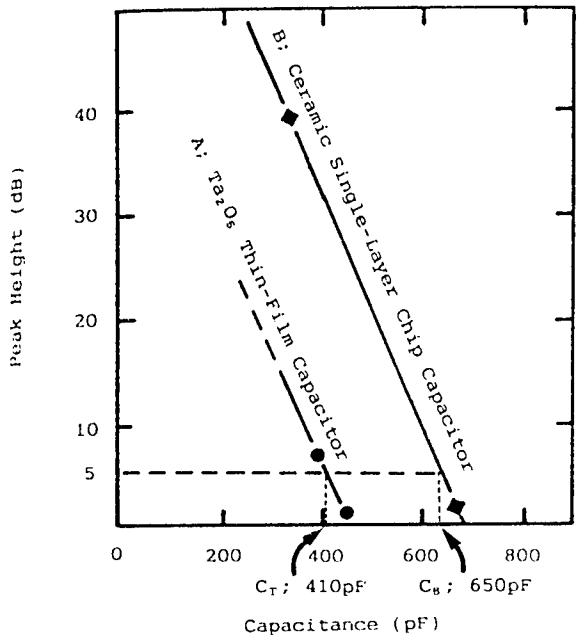


Fig.7 Comparison Of The Osillating Peak Heights Between The Ta_2O_5 Thin Film Capacitor And The Ceramic Single-Layer Chip Capacitor

shows the relations between the peak heights and the capacitances. The peak heights of the two Ta_2O_5 thin-film capacitors draw one straight line; A, and also those of the two ceramic single-layer chip capacitors draw another; B in Fig.7. The two lines (A and B) are almost parallel.

Fig.7 shows that the higher the capacitance is, the lower the peak height is. Supposing that the peak heights was reduced to 5dB, the capacitances which can be determined from each dielectric's lines would be different. From the A line, the capacitance of the Ta_2O_5 thin-film capacitor is about 410pF. From the B line, that of the ceramic single-layer chip capacitor is about 650pF. In other words, the capacitance of the Ta_2O_5 thin-film capacitor corresponds with 60% of the ceramic single-layer chip capacitor's, in order to reduce the oscillating peak height to 5dB at about 150MHz.

CONCLUSION

We have developed a Ta_2O_5 thin-film capacitor which is compatible with die-bonding by Au-Si solder and hermetic glass-sealed packaging. Its lower and upper electrodes are a metal plate and a metal thin film, respectively. This report described a Ta_2O_5 thin-film capacitor which used the rolled sheet of Fe-42%Ni alloy as the metal plate, and Al as the metal thin film. The thermal coefficient of capacitance is less than 400ppm/deg. in the range of 25℃ to 150℃. The change of capacitance by frequency is very small in the range of 1MHz to 1GHz. The $\tan\delta$ is less than 0.5% at 1MHz. This capacitor can withstand a temperature of 500℃ for more than ten minutes.

We compared its capacitance change against the frequency with the $BaTiO_3$ base ceramic single-layer chip capacitor's, and measured the gain of an amplifier which was composed of an amplifier IC chip and a capacitor in a leadless chip carrier package. The capacitance of the $BaTiO_3$ base ceramic single-layer chip capacitor was decreased to about 60%, thereby its performance as a by-pass capacitor was lost at 150MHz. And then its capacitance became negligible above 400MHz. The Ta_2O_5 thin-film capacitor maintained nearly constant capacitance up to 1GHz. Incorporating a Ta_2O_5 thin-film capacitor into the IC package was confirmed to be a more effective decoupling technique, particularly at more than 100MHz. The measurement and the analysis of the capacitance at higher frequency range are subjects of the future study. The applications of this new type capacitor for the packaging of the high speed and high performane IC's are expected to expand. They will become increasingly important for achieving greater compactness, higher speeds and improved functions of today's rapidly abvancing electronic appliances and systems.

ACKNOWLEDGMENTS

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DEVELOPMENT OF THIN FILM RESISTOR AND ABRASION PROTECTIVE LAYER FOR THERMAL PRINTING HEAD

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Abstract

Newly developed double layer resistor formed by RF sputtering method and abrasion protective layer formed by plasma CVD method are described in this paper. Si/(Ti-C-Si-O) double layer resistor has high resistvity, low temperature coefficient of resistance (TCR) and high resistance for thermal oxidation. And, SiON abrasion protective layer formed by plasma CVD method using SiH_4-N_2-N_2O gas mixture at temperatures more than 350 °c has high micro-hardness,high thermal durability and high productivity. Highly reliable,highly productive and high resistance thermal printing head was realized by using these materials.

Introduction

Printing technology has been used in facsimile equipments,ticket machines,computer terminals,video printers and various other appliances. Among various kinds of non-impact printing techniques, thermal printing is the most popular method, because of its maintenance free structure,compactness and low cost printing. The thermal printing is desired to satisfy a higher resolution,a higher printing speed,a lower printing energy and lower appliance cost. So,the thermal printing head ,which plays the most important role in thermal printing,has been developed powerfully,but it has not been able to satisfy the requirements mentioned above.

Two different methods have been known for producing the thermal printing head, namely a thick film type thermal printing head[1] and a thin film type thermal printing head[2]. Although a thin film type thermal printing head has a higher resolution and a lower printing energy than a thick film type thermal printing head,its productivity is not so good as that one. This disadvantage is probably attributable to the production method of protective layer of heat elements. The abrasion protective layer with near 5 μm thick and the oxidation protective layer coated under the abrasion protective layer have been formed by RF sputtering method. Generally,the insulating films formed by RF sputtering method have low deposition rate. Therefore, the developments of the resistor materials with a high resistance for oxidation and the abrasion protective materials with high productivity are very important for a thin film type thermal printing head . In oder to obtain a high stability resistor film and high productivity of abrasion protective layer, we studied Si/(Ti-C-Si-O) double layer resistor formed by RF sputtering method and SiON abrasion protective layer formed by plasma CVD method.

Characteristics of resistor film

The structure of thermal printing head is shown in Fig.1. This thermal printing head consists of multi-layer films and is constructed through photolithographic technique. Heating elements are composed of high resistivity materials. Ti-C-Si-O RF sputtered thin films give a sufficiently high resistance. The high resistance permits high quality and low printing energy. Fig.2 shows resistivity and temperature coefficient of resistance (TCR) for the as-sputtered Ti-C-Si-O films as a function of SiO_2 content in the targets. Resistivity increased with increasing SiO_2 content in the target. On the other hand, TCR changed from positive to negative values with increasing SiO_2 content in the target. This film has high resistivity (near $5.6\times10^{-5}\,\Omega\cdot m$) and low TCR (less than -500 ppm/ °c).

The annealing effect on electrical and structual characteristics was investigated, using Si/(Ti-C-Si-O) double layer resistor deposited on a glazed alumina substrate. 1 hour annealing was carried out in an air environment. Sheet resistance changes at various annealing temperatures are shown in Fig.3 as a function of Si film thickness. The amount of the change in sheet resistance was expressed as a normalized figure to the initial sheet resistance value. The characteristics of sheet resistance change in this test largly depended on Si film thickness in the Si/(Ti-C-Si-O) double layer resistor. The sheet resistance of Ti-C-Si-O single layer resistor changed very high values at temperatures more than 300 °c, nevertheless Si/(Ti-C-Si-O) double layer resistor with only 6 nm thick Si film had a high resistance for thermal oxidation. Auger analysis showed that the high resistance for thermal oxidation was attributable to Si film stability. Fig.4 shows the results of Auger depth profile with the as-sputtered resistor film and the annealed resistor film. Auger depth profile of Ti-C-Si-O layer did not change before and after annealing. Thus,it was recognized that Si film had remarkable effect for the oxidation protective layer. Fig.5 is the results of the sheet resistance changes at various sheet resistance films as a parameter of Si film thickness. At Ti-C-Si-O single layer resistor, the more the initial sheet resistance became higher values, the more the sheet resistance changes were very large. On the other hand, Si/(Ti-C-Si-O) double layer resistor was found to have strong resistance against thermal oxidation regardless of the sheet resistance values.

The contact resistance was investigated after depositing electrode films on Si/(Ti-C-Si-O) double layer resistor,because Si film had a high resistivity.

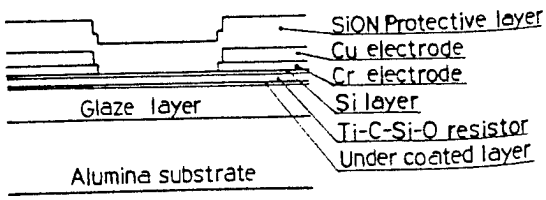


Fig.1 Structure of heat elment

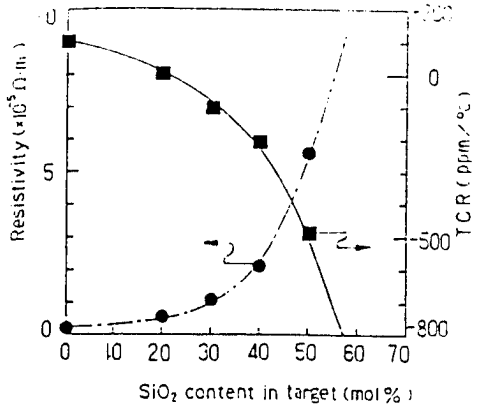


Fig.2 Resistivity and TCR VS. SiO_2 content in target

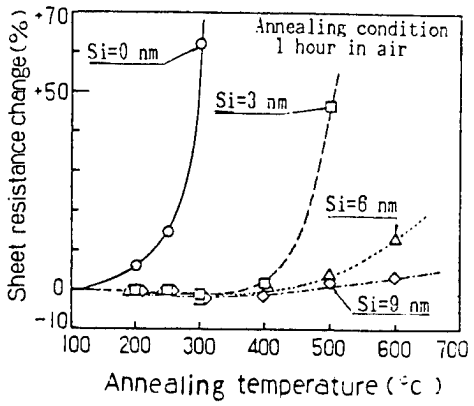
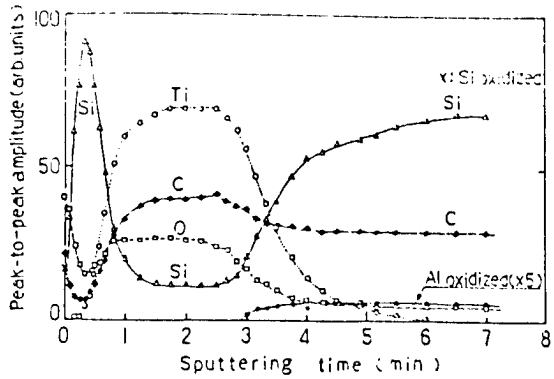
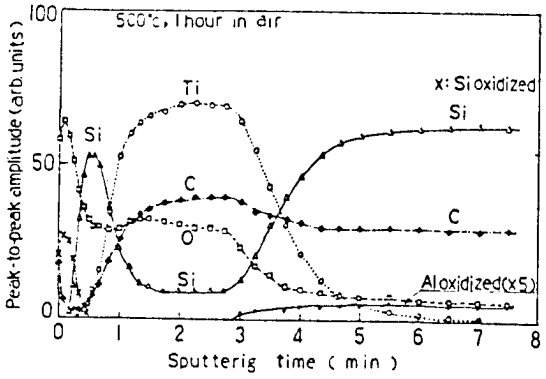


Fig.3 Sheet resistance change VS. annealing temperature



(A) As-sputtered film



(B) Annealed film

Fig.4 Auger depth profile of the as-sputtered film and the annealed film

Fig.6 is the results of the resistance values of thermal printing head with the sheet resistance of Si/(Ti-C-Si-O) double layer. The sizes of heat elements of these thermal printing heads are 105 μm wide and 175 μm long. So, these results shown in Fig.6 were recognized that the contact resistance values were nearly zero ohm, when Si film thickness was less than 12 nm.

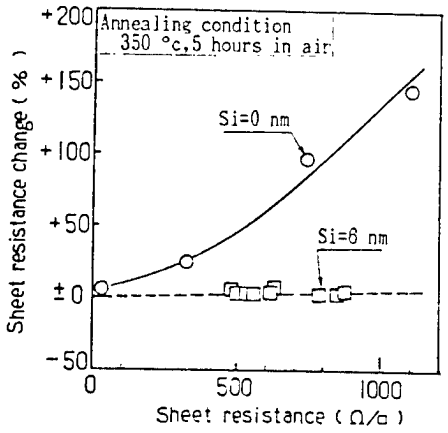


Fig.5 Results of sheet resistance change VS. initial sheet resistance

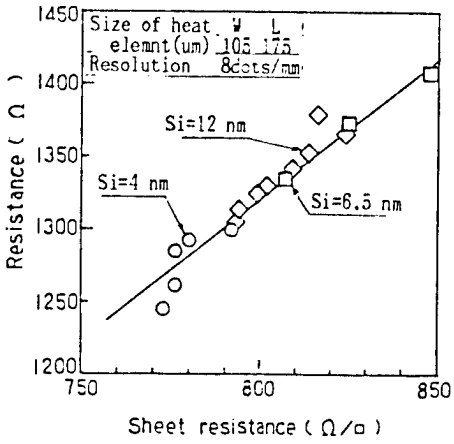


Fig.6 Resistance values VS. sheet resistance

Chracteristics of abrasion protective layer

Generally, conventional printing element surface protective layer is composed of double layer of SiO_2 (2~3 μm) sputtered film and Ta_2O_5 (3~5 μm) sputtered film[3]. As the insulating films formed by sputtering method have low deposition rate, the productivity is not so good. As mentioned above, Si/(Ti-C-Si-O) double layer resistor has a high resistance against thermal oxidation. According to this result, the oxidation protective film (SiO_2) is not necessary. Plasma CVD method has advantages of low substrate temperature and large deposition area. However the method has a disadvantage of difficulty of production. Silicon nitride (SiN) films formed by plasma CVD method have been used for the application in semiconductor fabrication. However, there are some problems on thermal stability, cracking resistance, adhesive properties to other materials and large internal stress.[4][5] Accoding to these disadvantages, Silicon nitride films can not be used for protective layer of thermal printing head. Silicon oxynitride (SiON) films prepared by plasma CVD method using SiH_4, N_2 and N_2O gas mixture were investigated for protective layer of a thermal printing head, because SiON films had less hydrogen contamination, high thermal stability and small internal stress. Fig.7 shows the deposition rate (DR), internal stress (σ) and micro-hardness (Hv) of SiON films as a function of N_2O gas flow rate. Internal stress measurements were performed by measuring the bending of about 5 μm thick oxynitride-coated Si wafer with an flatness tester. Micro-hardness of about 5 μm thick films deposited on a glazed alumina substrate was measured with Micro Vickers diamond indenter at a load 25 gf. Although the deposition rate increased as N_2O gas flow rate increased, the internal stress and the micro-hardness decreased with increasing N_2O gas flow rate.

Fig.8 is the results of micro-hardness and internal stress with a substrate temperature. The internal stress gradually decreased with raising a substrate temperature. On the other hand, the micro-hardness linearly increased

with raising a substrate temperature. These results show that SiON film has enough hardness and stability as a protective layer for a thermal printing head. In oder to explain the experimental data given above, the composition of the SiON films was investigated. Fig.9 is the results of the composition of silicon,oxygen and nitrogen, and hydrogen concentration of SiON films deposited at 400 °c, as a function of a N_2O gas flow rate. The composition of silicon,oxygen and nitrogen was measured by X-ray photoelectron spectroscopy (XPS) and Rutherford back scattering (RBS), and hydrogen concentration was measured by Infraed absorption spectrophotometry (IR) and Secondary ion mass spectrometry (SIMS). According to this figure, the composition of silicon and nitrogen decreased with increasing a N_2O gas flow rate, and the composition of oxygen increased with increasing a N_2O gas flow rate. But, hydrogen concentration did not change with a N_2O gas flow rate. It was recognized that SiON film changed from SiN rich film to SiO rich film with increasing a N_2O gas flow rate. Fig.10 is the results of the composition of silicon,oxygen and nitrogen, and hydrogen concentration of SiON films as a function of a substrate temperature. The composition of nitrogen tended to increase,but the composition of oxygen tended to decrease with raising a substrate temperature.

Although these results were not clear, hydrogen concentration clearly decreased with raising a substrate temperature. It was recognized that SiON films became high density with raising a substrate temperature.

Chracteristics of a thermal printing head

Chracteristics of a thermal printing head prepared by newly developed resistor and abrasion protective layer (SiON head) were invesitigated. Fig.11 shows a pulse durability of SiON head with input power. A durability test was performed as follows. Whenever the heat elements were applied fixed number pulses with 1 ms heat pulse and 10 ms heat repetition interval in constant electric power, the resistance of the heat elements were measured automatically. This measurement cycle was continued,untill the resistance of the heat elements changed over 5 % for the initial resistance of each heat element. A pulse durability was dignified as the pulse numbers being applied the heat elements, when the resistance of a heat element changed over 5 % for initial resistance. Horizontal axis represented normalized power, which was normalized to the power for obtaining optical density OD=1.2. For comparison, a pulse durability of a thermal printing head with silicon carbide abrasion protective layer (SiC head) was investigated. When the silicon oxynitride protective layer was formed at temperatures more than 350 °c, SiON head had more excellent durability than SiC head.

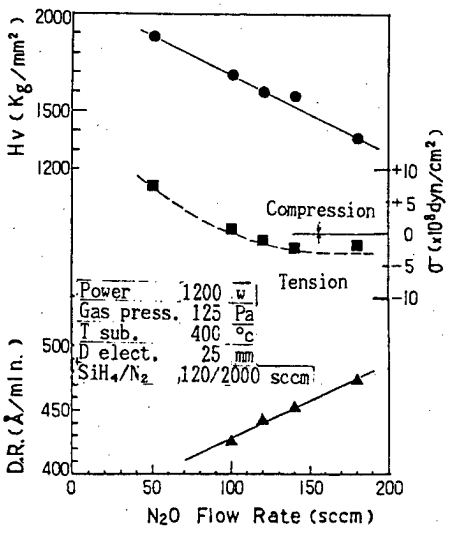


Fig.7 Deposition rate (DR),internal stress (σ) and microhardness of SiON films VS. N_2O gas flow rate

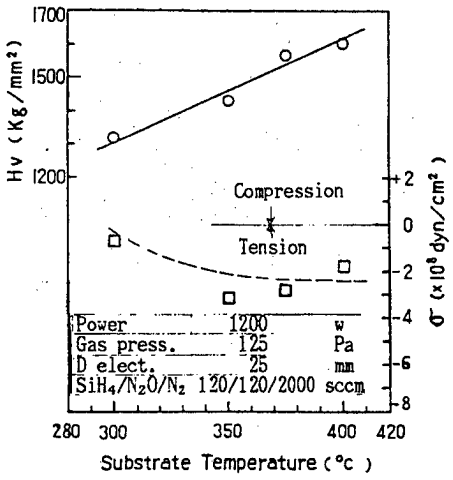


Fig.8 Internal stress (σ) and micro-hardness (Hv) of SiON films VS. substrate temperature

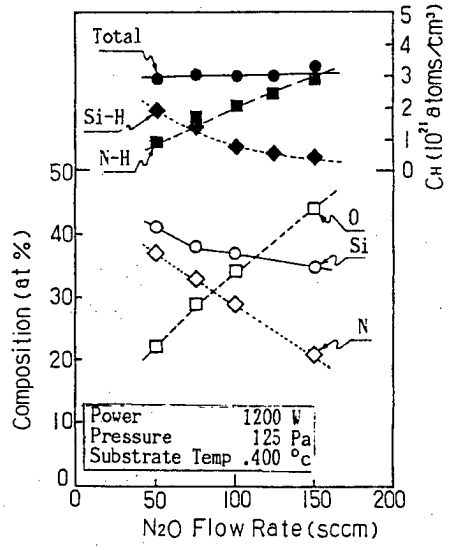


Fig.9 Composition of SiON films VS. N_2O gas flow rate

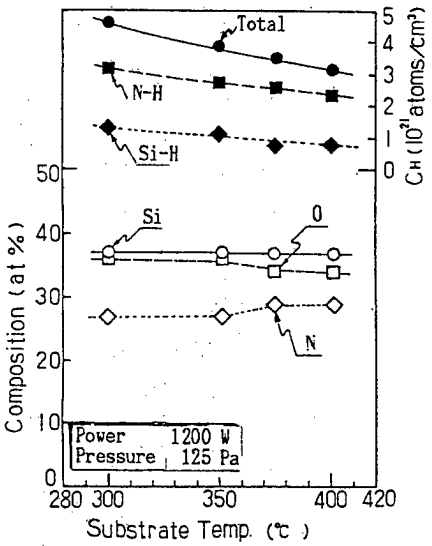


Fig.10 Composition of SiON films VS. substrate temperature

Fig. 12 is the results of optical density with input power. In this figure, SiON head and SiC head were measured. Printing powers of both heads for obtaining optical density OD=1.2 were 0.31 w/mm² with 1 ms heat pulse and 0.62 w/mm² with 0.5 ms heat pulse. But,the dot patterns printed by using SiON head were a little different from the dot patterns printed by using SiC head. Fig. 13 shows the results of printed examples. It was realized that more excellent dot patterns were printed by using SiON head.

To ensure durability of a thermal printing head, it is necessary to ensure not only a heat pulse durability of the heat elements, but also an abrasion resistance durability. Fig.14 shows the results of the abrasion resistance measurement. The micro-hardness of SiC protective layer and SiON protective layer were shown in Table 1 . Although the micro-hardness of SiON protective layer was smaller than the micro-hardness of SiC protective layer, the abrasion resistance of SiON protective layer was a little more excellent than SiC protective layer. The abrasion resistance of both layers were enough small to ensure a distance of 30 km for printing life.

Conclusion

High resistance and stability thin film resistors prepared by RF sputtering method and the abrasion protective layer formed by plasma CVD method have been developed. The newly developed resistor layer has double layer structure of Si/(Ti-C-Si-O) films. This resistor layer shows strong resistance to thermal oxidation regardless of the sheet resistance. Silicon oxynitride protective layer formed by plasma CVD method with SiH_4, N_2 and N_2O gas mixture has enough hardness and stability to use for the abrasion protective layer of a thermal printing head. Chracteristics of a thermal printing head with newly developed resistor and abrasion protective layer have excellent printing, high resistance and high productvity.

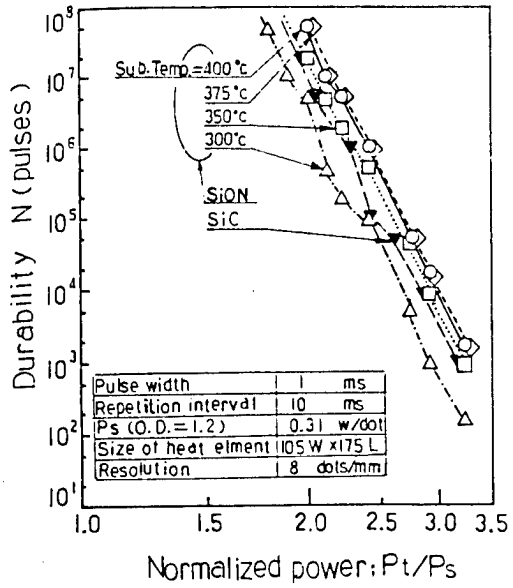


Fig.11 Result of pulse durability measurement

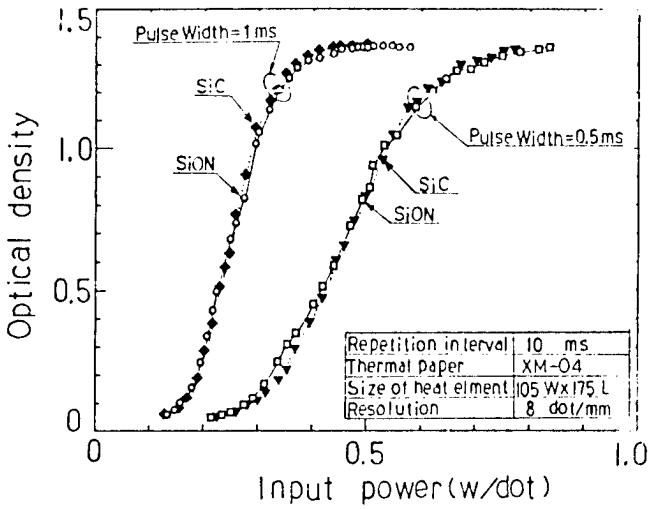


Fig.12 Result of optical density measurement

(A) SiC head (B) SiON head

Fig.13 Printing examples made by using thermal printing heads with (A) SiC head and (B) SiON head

Table 1 Micro-hardness of SiC,SiON

	micro-hardness
SiC	2500 kg/mm²
SiON	1500 kg/mm²

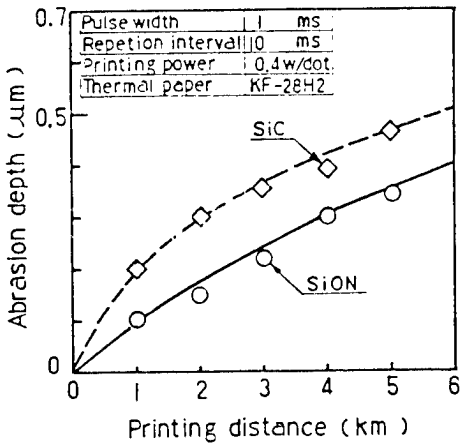


Fig.14 Result of abrasion resistance measurement

Acknowledgement

The authers wish to thank Dr.K.Wasa, Dr.T.Nagata and Mr.H.Ohtani for their guidance and encouragement throughout this work.

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APPLICATION OF ALUMINUM-ALLOY ULTRAHIGH VACUUM SYSTEM TO SEMICONDUCTOR DEVICE FABRICATION PROCESSES

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ABSTRACT

The aluminum-alloy ultrahigh vacuum (UHV) system possesses several excellent vacuum properties such as an extremely low outgassing rate or an extremely short pumpdown time to reach UHV region. It has, therefore, a considerable potential as a UHV system used in the next generation semiconductor processes. For this employment, however, proper surface treatments must be made on the inner surface of the chamber according to the environment of the processes. A lathing method which utilizes alcohols as the lathing liquid has been developed for this purpose and found to be effective for processes which do not contain corrosive species. A silicon molecular beam epitaxy (MBE) chamber has been constructed with this method and its vacuum properties were tested. For processes which contains corrosive species, a kind of ceramic coating was tested to be found operative.

1. Introduction

Semiconductor device fabrication processes, in response to demands toward both higher operation speed and ultralarge scale integration (ULSI) of the devices, now need higher purity of source materials and higher cleanliness of its environment. This is because the whole fabrication process for such devices become much more fragile against contamination of small particles or impurity atoms, causing a re-examination of the conventional criterion for the degree of cleanliness. Following this trends toward ultimate purity and cleanliness, semiconductor processes now seek to employ ultrahigh vacuum (UHV) systems as their basic technology.

In order for UHV systems to be employed in factories, it is important that they possess enough compatibility with conventional systems in the present processing line. In other words, accessibility to UHV world is the key point in promoting the installation of UHV into the process. Aluminum-alloy UHV system is one of the promising candidates for such practical UHV systems. It was originally developed as a UHV system for high energy particle accelerators which features its extremely low residual radioactivities [1]. During the course of the development, however, aluminum-alloy UHV system was found to possess an excellent by-product in that it exhibits an extremely low outgassing rate or extremely short pumpdown time to reach UHV region with very reduced or even without bakeout procedures. Besides, it is (1) composed of completely non-magnetic metal of high-purity, (2) light in weight, and (3) economical in cost. These features clearly meet the above requirements for the UHV system in semiconductor processes. In Table I, advantages and disadvantages of the aluminum-alloy UHV system are listed. All the disadvantages can be bypassed and benefits of the advantages overcompensate the disadvantages.

Table I Advantages and disadvantages of aluminum-alloy UHV system

Advantages

1)Low residual radioactivity
2)Low outgassing rate
3)High thermal conductivity
4)Completely non-magnetic
5)No thermal modification at ultralow temperatures
6)Various alloys available
7)Hardness control by heat treatments or mechanical treatments
8)Complicated profile available by extrusion using various porthole dies
9)Various machining techniques available such as pressing, rolling, bulging, or warm die forging
10)Various surface treatments available such as alumite-treatment, ion-plating, or ceramic-coating
11)Light weight and large specific strength
12)Heavy metal elements free
13)Low overall cost

Disadvantage

1)Low melting point
2)Low mechanical strength
3)Low tolerance against corrosion
4)Difficulties in welding
5)Limited available vacuum components

Aluminum-alloy UHV system consists of several element technologies: (1) [illegible] of aluminum-alloys, (2)conflat compatible aluminum-alloy flanges, (3)aluminum-alloy bolt-nut system, (4)machining method, (5)cleaning method, (6)welding method, (7)surface treatment method, and (8)development of aluminum-alloy vacuum components. Although not any one of the above elements is indispensable, the seventh technology, surface treatment method, is of substantial importance. Namely, in order to take full advantage of the above excellent vacuum properties of the aluminum-alloy UHV system, a proper surface treatment must be made on the inner surface of the aluminum-alloy chamber according to the process to which the system is to be installed. This paper is devoted to describe the adaptability of the aluminum-alloy UHV system to semiconductor processes with emphasis on the importance of surface treatments.

2. Surface treatments

The largest reason that aluminum and its alloys have long been considered inappropriate as UHV materials is a lack of proper surface treatments. Aluminum and its alloys as their extruded state are covered with a thick (>100A), porous oxide-hydride film which forms an enormous source for outgassing species. Noticing this point, Ishimaru [1] has developed a so-called special extrusion process [illegible] the inner surface of the pipe is exposed only to a mixture gas of pure oxygen and argon during the extrusion. This process greatly reduced the thickness of the surface oxide layer to about 25 A, and a chamber made with this method showed a remarkably low outgassing rate of some 10^{-14} Torr 1/s cm^2.

Table II shows a list of existing surface treatments for aluminum-alloys. First five of the six methods are to produce a thin, clean oxide layer on the metal surface. Lathing processes were developed to obtain such surfaces on pipes of larger diameters or on slabs. The last method, ceramic coating, is for use in reactive processes in which chemical species are introduced. In what follows, our results on (A)ethanol lathing process, (B)isopropanol lathing process, and (C)ceramic coating process are given.

Table II Surface treatments used in aluminum-alloy UHV system

Special extrusion process (EX extrusion)	
Special lathing process (EX process)	
Ethanol lathing process (EL process)	....present work
Isopropanol lathing process (IPL process)	....present work
EX-baking process	
Ceramic coating	....present work

(A)Ethanol lathing process (EL process)

Ethanol lathing [2] is a method in which inner surface of the chamber is lathed using pure ethanol as a lathing liquid. A depth profile measurement of the Auger electron spectroscopy (AES) for this surface shows that the oxide thickness is reduced to about one-sixth of that of native oxide by lathing. The outgassing rate from this surface has been measured by a throughput method (Fig. 1). The volume and the inner surface area of the test chamber were 64 l and $1x10^4$ cm^2, respectively. Before the pumping the chamber had been pumped to UHV region and exposed to air for about 1 h. After 24 h of evacuation the outgassing rate reached the order of 10^{-11} Torr 1/s cm^2. The chamber was then baked at about 100 C for 45 h. After the bakeout the outgassing rate was lowered by two orders of magnitude to a value of $1x10^{-13}$ Torr 1/s cm^2. This value is one to two orders of magnitude smaller than that for stainless steel. It is worth noting that a bakeout as low as at 100 C is sufficient in producing this extremely low outgassing rate. The long bakeout time duration adopted here was to confirm the saturation in outgassing rate during the bakeout. As shown later a much shorter bakeout time drives the chamber to ultrahigh vacuum region.

Figure 2 shows the pumping curve for the same chamber. As shown schematically in the inset, the pumping system consists of both a turbomolecular pump (50 1/s), backed up with an oil diffusion pump (DP) and a titanium sublimation pump mounted in a liquid-nitrogen-shroud. In 2 h of evacuation from atmospheric pressure the chamber can be pumped down to the order of 10^{-7} Torr, and in 5 h to the order of 10^{-8} Torr. At about 20 h after the start of evacuation liquid nitrogen was introduced to the shroud, which drives the system to the order of 10^{-10} Torr. The ultimate pressure with this configuration was $7.4x10^{-10}$ Torr which was accomplished in 24 h of evacuation. It must be emphasized that the above result is obtained with no bakeout procedures.

In actual semiconductor processes, there might arise some needs for UHV systems to reach ultrahigh vacuum, say the order of 10^{-10} Torr, in several hours. Figure 3 demonstrates the capability of this operation. Initially, the chamber had been exposed to air (moisture=70%) for 1 h. After 30 min of pumping down, the baking heater was switched on for 1.5 h in which the chamber temperature rose to 88 C. At about 1.75h after the baking heater was switched off, when the chamber was cooled down to 27 C, liquid nitrogen was introduced to the titanium sublimation pump (TSP) shroud and the pressure reached the order of 10^{-10} Torr in 6h and 20 min after initial pumpdown.

(B)Isopropanol lathing process (IPL process)

In ethanol lathing process, the aluminum-alloy metallic surface exposed by the machining immediately interacts with ethanol molecules. Tindall et al[3] showed that methanol molecules in contact with the aluminum clean surface cause an oxidation of the surface at room temperatures and an additional heating up to 450 K causes a formation of an amorphous carbon layer at the top surface. If a similar mechanism is functional at the liquid-solid interface of the ethanol-aluminum system, a possibility arises that a carbon-containing surface oxide layer is formed during the ethanol lathing procedure. Such oxide layers, being heated or impinged by molecules, ions or photons, would produce carbon oxides or other carbon-containing molecules, which would be harmful in realizing clean, extreme ultrahigh vacuums.

On this background, we investigated by x-ray photoemission spectroscopy (XPS) the carabon contents within the surface oxide layer formed by the ethanol lathing. We also investigated effects of using other alcohols in the treatment since the oxidation mechanism and hence the extent of carbon incorporation may differ according to the alcohol. Table III shows the surface carbon content and the oxide thickness for each alcohol. Carbon contnets are normalized with the integrated intensity of the Al2p peak in the bulk

for the same sample. Surface thicknesses were obtained from the intensity ratio of the oxide and metallic part of the Al2p peak. From the table one can see that the surface oxides become thinner as alcohols with larger molecular weight are used. On the other hand, carbon contents showed its minimum value at isopropanol lathed surface. Although the results are preliminary, we at present consider isopropanol an alternative to ethanol for its smaller surface oxide thickness, lower surface carbon contents, less volatility, all compared with the ethanol surface, and the least toxicity among all the alcohols which is liquid at room temperatures. Experiments on the outgassing rate from the isopropanol-lathed surface is now being prepared.

Table III Oxide thickness and Surface carbon content of surfaces lathed with various alcohols.

Alcohol	Oxide thickness(A)	Surface carbon content(a.u.)
methanol	24.9	....
ethanol	25.3	0.82
1-propanol	20.8	0.83
isopropanol	20.6	0.75
n-butanol	21.0	0.79
2-butanol	19.5	0.82
isobutanol	17.8	0.83

(C)Ceramic coating

For processes which utilize reactive species, a protective surface treatment must be made. A kind of ceramic coating has been found to be effective for this purpose [4]. Fig. 4 shows outgassing rates from three different surfaces before and after an exposure to dichlorosilane (100%, 1.4atm.) for 10 days. Before the exposure, both ethanol lathing (EL) and special extrusion (EX) samples showed equivalent low outgassing rates whereas the ceramic coating (CC) showed about four times larger outgassing rate. On introducing the reactive gas, however, the order is reversed and the outgassing of the former two became four times larger than the latter. This ceramic coating possesses almost as low outgassing properties after sufficient baking as a UHV surface treatment. Therefore, for aluminum-alloy UHV systems into which reactive species are to be introduced, use of ceramic-coating is strongly suggested. It is especially useful for GaAs MBE chambers since it shows a perfect protection against corrosion caused by an interaction between gallium and aluminum [5].

3.Application to semiconductor processes

Aluminum-alloy UHV is successfully applied in our laboratory to silicon molecular beam epitaxy (MBE) system. The inner surface of the chamber has been finished with the EL process. In this MBE system, monosilane(SiH_4) gas source is used as a molecular beam source. Hence, the working pressure of 5×10^{-5} Torr is totally composed of silane molecules. In spite of this rather high working pressure of the process, it turned out that an attainment of UHV region in the base pressure is critical for obtaining qualified growth films. The system can be pumped down from the atmospheric pressure to its base pressure of 4×10^{-10} Torr in 14 hours including a 140 C, 10-h bakeout. Therefore, growth experiments can routinely operated once a day although the lack of load-locks forces us to purge the growth chamber with dry nitrogen after growth to exchange samples. The high thermal conductivity of the material, in addition to its low outgassing rate, also contributes in attaining this short pump down time since it brings about high uniformity in the bakeout and an extremely short cool-down time.

4. Conclusion

The aluminum-alloy UHV system possess excellent vacuum properties in that it requires very short pumpdown time to reach UHV region with very reduced or even without bakeout procedures. Coupled with its reduced weight and low cost, these merits suggest its potentiality as a UHV system in next generation semiconductor processes. As an important part of this vacuum technology, several surface treatments have been developed or tested to confirm above excellent vacuum properties under actual circumstances. Aluminum-alloy UHV systems with properly processed surfaces provides us with a remarkably convenient tool to access UHV region and its application to variety of production processes are expected.

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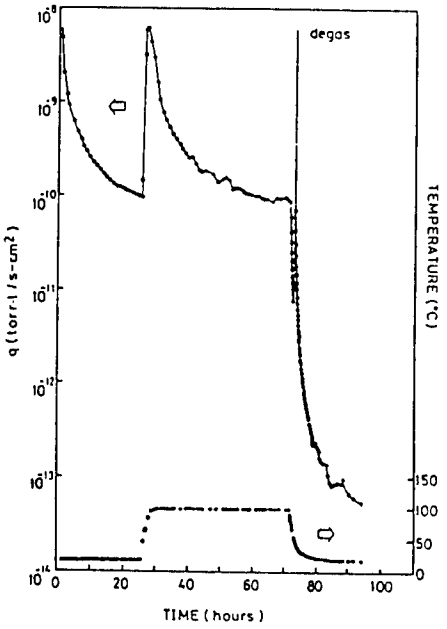

Fig. 1 The outgassing rate of an EL-processed chamber.

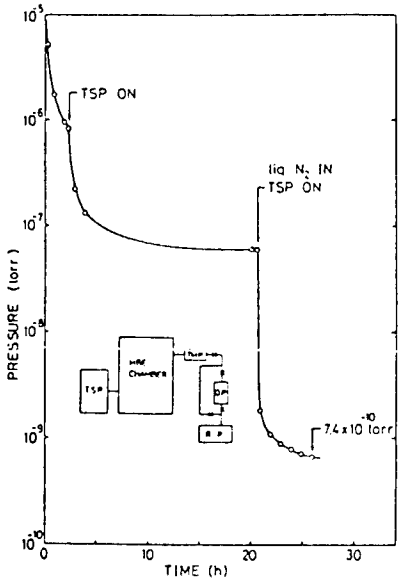

Fig. 2 Pumpdown curve without bakeout.

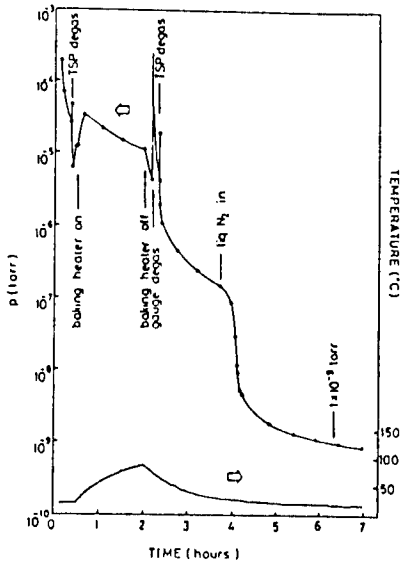

Fig. 3 Pumpdown curve with 1.5-h bake-out.

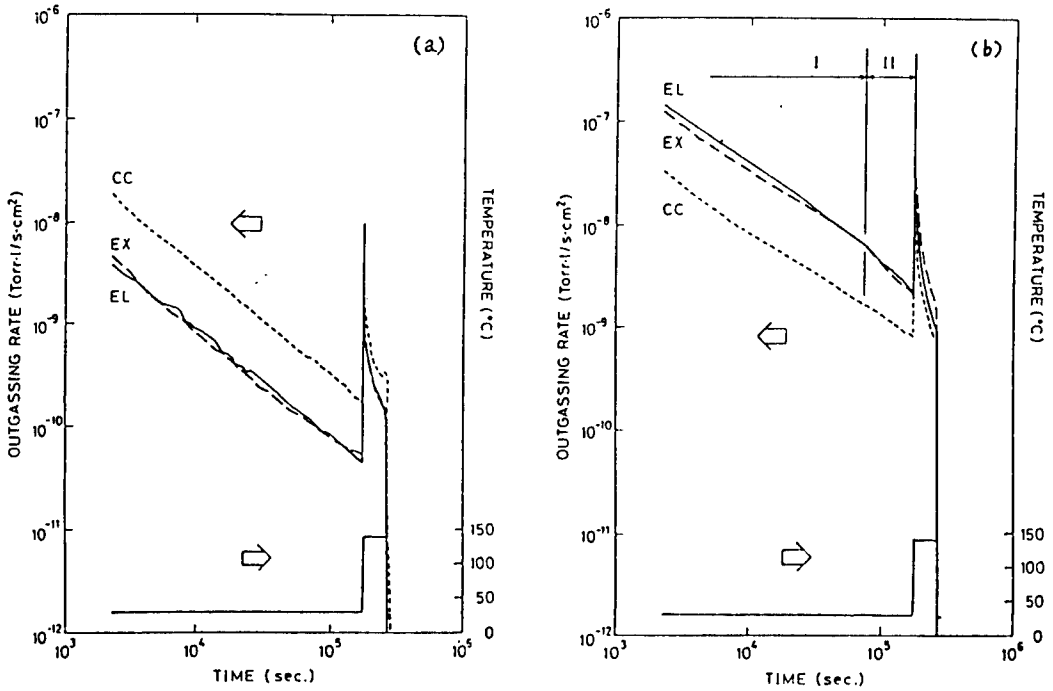

Fig. 4 (a)Outgassing rates for the as-received surfaces of specially-extruded (EX), ethanol-lathed (EL), and ceramic-coated (CC) A6063 pipes. (b)Outgassing rates after a 1.4 atm, 10-days exposure to dichlorosilane.

DEVELOPMENT OF A FORCE SENSOR FOR MINUTE LOAD MEASUREMENT

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ABSTRACT

A force sensor has been developed for a minute load measurement. It consists of a load sensing part, with a piezoresistive silicon diaphragm sensor, and a load conducting part. The actuator, as a load conductor, combined with a gimbal leaf-spring, transmits a part of the applied force onto the diaphragm surface with no friction. Its maximum displacement is restricted by the spacer to prevent the thin diaphragm from breaking. The mechanical parts were assembled in a micron order, yielding the conducting part, by using a diffusion welding process.

The developed force sensor achieved 19.4 mV/gf force sensitivity in a 70 gf load range, and saturation characteristic for over 70 gf load.

1. INTRODUCTION

Developing a sensor for a minute load is one of the key factors, not only in achieving artificial intelligence and an automation system, but also in improving accuracy and reliability for industrial instrumentations in various fields, such as precision equipments, medical instruments and robotics. Conventional force sensors, used to detect a rather large load, are large in size and a relatively small sensitivity. Therefore, they can hardly be used to measure a minute load precisely.

Recently, the authors have developed a new kind of force sensor[1] based on the piezoresistance effect. The force sensor sensing elements are formed into the silicon wafer, using conventional silicon IC processing technologies. Furthermore, the sensor has a thin leaf-spring, which can share most of an applied load. Thus it can control the sensitivity by varying the spring stiffness. In sensor assembling process, diffusion welding[2] was introduced, allowing the many mechanical parts, such as the leaf-spring, an actuator and spacer to be joined precisely in micron order. In this paper, the sensor structure, the force sensing element, the leaf-spring, and the typical transfer characteristics will be presented.

2. FORCE SENSOR

A silicon diaphragm piezoresistive sensor utilizes the excellent mechanical characteristic for silicon, as well as electrical characteristics[3]. The silicon diaphragm has greater stiffness than various metals. Moreover, it has no hysteresis, since it is made of a silicon single crystal with excellent elasticity. Therefore, it has good repetitive motion characteristics, with no fatigue phenomenon appearing.

The diaphragm can be deflected[4], not only by a uniformly distributed load, like a fluid pressure, but also by a concentrated load. A centrally applied concentrated load is chosen for the force sensor, described here, and the diaphragm is deflected directly by the applied load.

Figure 1 shows a cross sectional view of the developed force sensor. The force sensor can be roughly divided into two parts: A load sensing part and a load conductive part. The load sensing part consists of a silicon diaphragm sensor, a header on which the sensor is to be mounted, and an adjusting ring. The header is tightly inserted into the adjusting ring, which can be used to adjust the sensor setting height. On the other hand, the load conductive part consists of an actuator, a leaf-spring, a spacer and a housing. The leaf-spring was fabricated by a photo-etching process. A diffusion welding process was introduced to precisely join individual parts in a micron order. The actuator transmits an applied load to the top of the diaphragm center. The leaf-spring, welded to both the actuator and the housing, supports the actuator. Its stiffness controls the detected load range. The spacer, whose thickness was precisely controlled by grinding, was located under the leaf-spring to restrict the maximum leaf-spring deflection and to protect the diaphragm against an excessive load. The spacer was also welded to the leaf-spring and housing.

Main features of this force sensor structure are as follow: (1) No hysteresis can be found, due to no friction during sensing operation. That is because the actuator and the leaf-spring were joined together and actuated as one integral part, with no guide, such as a slide bearing. (2) The maximum deflection is strictly restricted

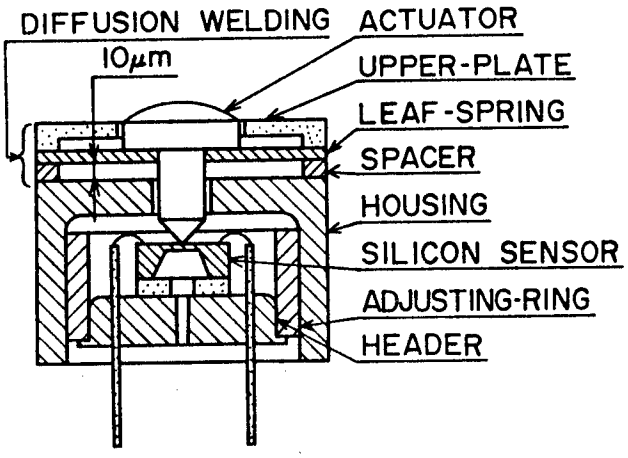


Fig.1. Cross sectional view of the developed force sensor.

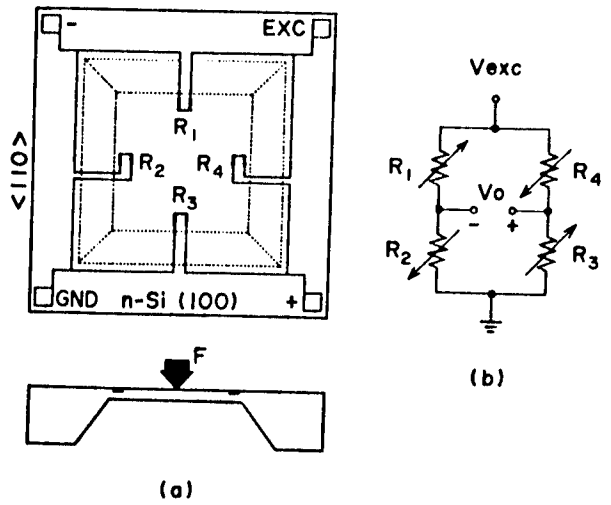


Fig.2. Piezoresistive silicon diaphragm sensor. (a) Sensor structure. (b) Bridge circuit with four piezoresistors.

by the spacer to prevent the thin diaphragm from breaking. (3) It is possible to design the sensor for different load ranges, from a minute load to a heavy load, by appropriately selecting the leaf-spring stiffness. This is because the applied load is divided into two parts, and that two divided loads are shared by the leaf-spring and the diaphragm.

3. SILICON DIAPHRAGM SENSOR

The piezoresistive silicon diaphragm sensor[5] is shown in Fig.2(a). It consists of a thin square silicon diaphragm, selectively etched from a much thicker wafer, and four piezoresistors (R1 - R4) diffused onto the diaphragm by ion implantation technology. The diaphragm measured 1 mm square and was $27\pm1\mu$m thick. The diaphragm surface was covered with an about 0.3μm thick SiO_2 layer, in order to protect piezoresistors against circumambient environment. As the diaphragm is quite thin, it is easily deflected by a load applied to its top or bottom. Such deflection changes the resistance of the piezoresistors, which is proportional to the applied load.

Each resistor is 20μm wide and 200μm long. The long side of each piezoresistors is laid out in the <110> crystallography direction on the diaphragm. R1 and R3 are perpendicular to the diaphragm edge, while R2 and R4 are parallel to the diaphragm edge. These two pairs are connected to form a wheatstone bridge circuit, excited by a constant voltage V_{exc}, as shown in Fig.2(b). An output voltage V_o is obtained in proportion to the load measured.

In order to calculate the diaphragm stiffness, diaphragm deflection, due to the concentrated force applied to the diaphragm center, is numerically evaluated by the Finite Element Method (FEM). Figure 3 shows the diaphragm center line displacement as a function of a distance from the diaphragm center. It is assumed that the diaphragm is 1 mm square and 20μm thick, and that the applied load is 10 gf. The center displacement shows that the spring constant for a 20 μm thick diaphragm is 2.1 gf/μm. Since the spring constant is in proportion to the cube of diaphragm thickness, the spring constant for the current diaphragm, 27μm thick, was calculated as

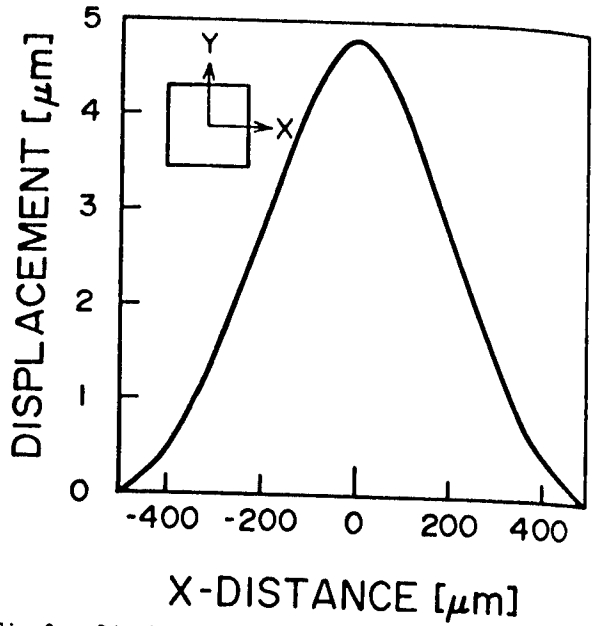


Fig.3. Diaphragm center line displacement as a function of distance from the diaphragm center. Concentrated applied load and diaphragm thickness are 10 gf and 20μm, respectively.

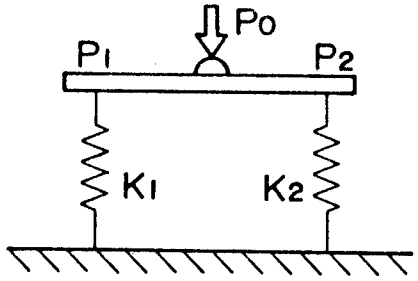
5.1 gf/μm. In addition, the breaking strength for the current diaphragm under a concentrated load, was measured, in order to obtain data regarding the maximum deflection in practical use. The diaphragm broke at 13μm displacement. Therefore, the maximum tolerance deflection in operation will be set at 10μm.

4. LEAF-SPRING

In the developed force sensor, the actuator, mechanically combined with the leaf-spring, always touches the silicon diaphragm surface. Therefore, it is actuated according to the leaf-spring deflection, and can move up and down freely, with no motion guide required. As a result, it is possible to eliminate hysteresis from the diaphragm motion and to improve repeatability as well as durability.

When applying the force sensor, for a variable load range, a spring constant should be altered to an appropriate value. A modeling diagram for a spring system in the sensor is shown in Fig.4. There are two springs, the leaf-spring and the diaphragm, in parallel. These two springs respectively pick up divided load, P_1 and P_2, from applied load P_0, according to their spring constants k_1 and k_2. As the diaphragm spring constant and maximum allowable deflection are 5.1 gf/μm and 10μm, respectively, as mentioned earlier, the maximum tolerance load for the fabricated diaphragm is calculated as 51 gf. If the maximum load applied is reduced to the same level as the diaphragm tolerable load, such as 51 gf, it is necessary to minimize the spring constant for the leaf-spring, to maintain sufficient sensitivity, while still retaining the actuator supporting function.

As the spring constant depends on the spring shape as well as the dimensions, there are many degrees of freedom which must be determined in order to design the spring. A thinner leaf-spring would be effective in reducing the spring constant. However, due to heat and pressure in



$K = K_1 + K_2$

Po : LOAD RATING

K : COMBINED SPRING CONSTANTS

K1 : SPRING CONSTANT [SILICON DIAPHRAGM]

K2 : SPRING CONSTANT [LEAF-SPRING]

Fig.4. Modeling diagram for a spring system in the force sensor.

the diffusion welding process, the circular plate, thinner than 150μm, would warp so much that it could not be applied for this purpose. The authors proposed the so called gimbal leaf-spring, as shown in Fig.5. Grooves in the thin metal plate reduce the spring constant without excessive warpage. Displacement dependences on applied loads, simulated by FEM, are shown in Fig.6. In the figure, three cases, gimbal springs with two different thicknesses and a circular plate, are compared. It can be seen that the displacement for the 250μm thick gimbal spring is more than ten times than that for the same thick circular plate. It was confirmed that the proposed gimbal structure was suitable for reducing the spring

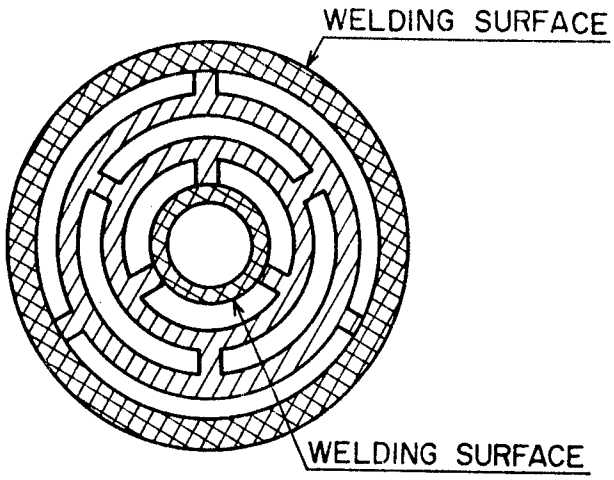


Fig.5. Gimbal leaf-spring structure.

constant. Moreover, spring constants for the proposed gimbal springs were 5.8 gf/μm and 1.3 gf/μm for 250μm and 150μm thicknesses, respectively.

In Fig.7, the combined whole spring constant, as well as individual constant components, are shown. As shown in the figure, the combination of a gimbal-spring 250μm thick and a silicon diaphragm 27μm thick offers the 10.9 gf/μm spring constant. Then, this combination is sufficient for use to detect a minute load, such as a few tens of a gram.

5. RESULTS AND DISCUSSIONS

The force sensor was assembled as follows: First, individual parts in the load conductive part were joined simultaneously by diffusion weld-

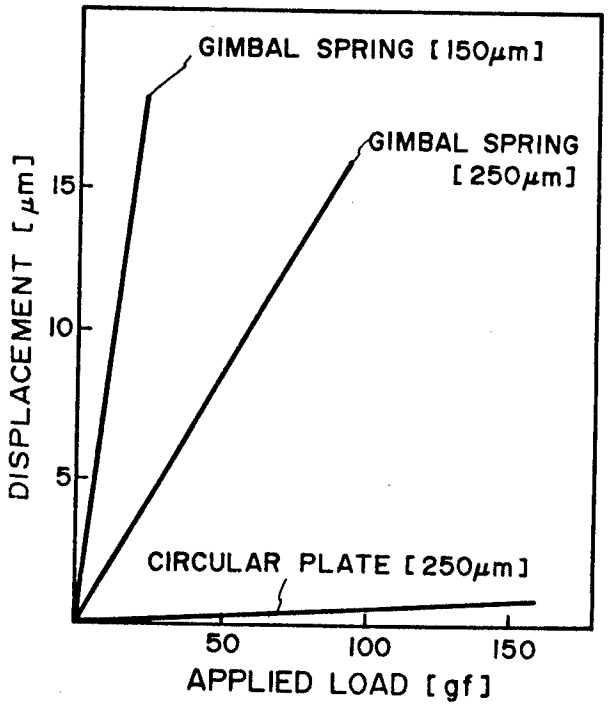


Fig.6. Displacement dependence on applied load for different springs.

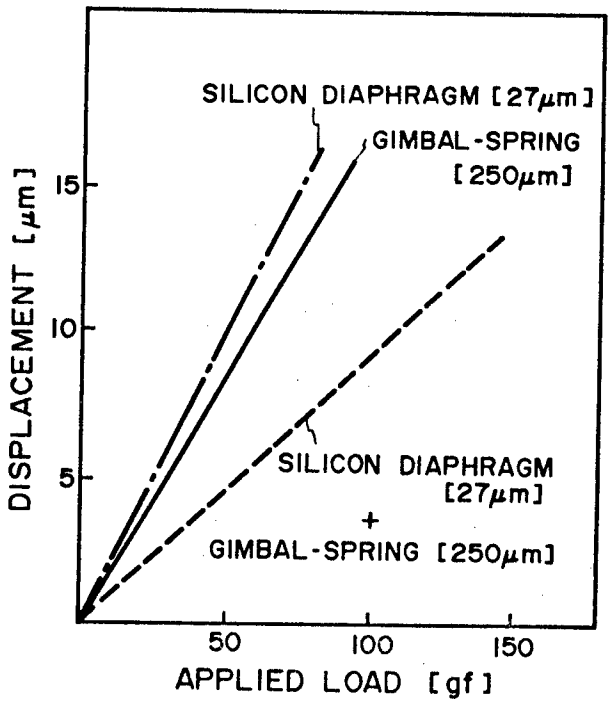


Fig.7. Displacement dependence on applied load for combined force sensor.

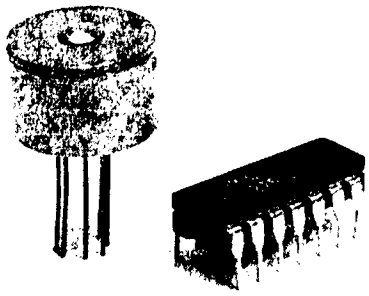


Fig.8. Fabricated force sensor photograph. A standard dual-in-line package is also shown for scale comparison.

ing, as mentioned before. Next, the sensing part was adhered to the housing after adjusting the diaphragm location, in order to retain the desired contact between the actuator and the diaphragm. The assembled force sensor is shown in Fig.8.

Figure 9 shows the measured transfer characteristics. The vertical axes show the output voltage and the diaphragm center displacement, while the horizontal axis shows the applied load. The sensor was excited by a constant 10 V. An output voltage as large as 1360 mV and a 9.2μm displacement were obtained for a 70 gf applied load. From the figure, the obtained output sensitivity was 19.4 mV/gf. Good linearity with no hysteresis was achieved. Also, the measured total spring constant, combined with the leaf-spring and the diaphragm, is 7.6 gf/μm, which agrees relatively well with the 10.9 gf/μm simulated value. These results indicate that the force sensor has sufficient sensitivity in a range where as much as 70 gf load is applied.

If the leaf-spring were thinned down, this force sensor could be used in a minute load application. The authors succeeded in making a leaf-spring thinned down to 150μm, and in joining the leaf-spring to a housing with little warpage, by using the welding process. When this leaf-spring, with a 1.3 gf/μm simulated spring constant, is combined with a sensing part having a 20μm thick diaphragm, as well as with a 2.1 gf/μm simulated constant, the total spring constant would become 3.4 gf/μm. This means that this sensor will measure a minute load, such as a 20 gf maximum load.

6. CONCLUSION

A force sensor suitable for a minute load measurement has been developed, utilizing a piezoresistive silicon diaphragm sensor. A concentrated detected load, transmitted by an actuator supported by a leaf-spring, was applied at the center of a diaphragm with no friction in operation. The diaphragm configuration is 27μm thick and 1 mm square. The maximum tolerance deflection for this diaphragm is limited to less than 10μm by the spacer, because the diaphragm breaks at 13μm displacement.

The leaf-spring stiffness is a design factor used to set the measurable load. In order to measure a minute load, less than 70 gf maximum load, a gimbal leaf-spring, with grooves in the spring plate, has been proposed to reduce its

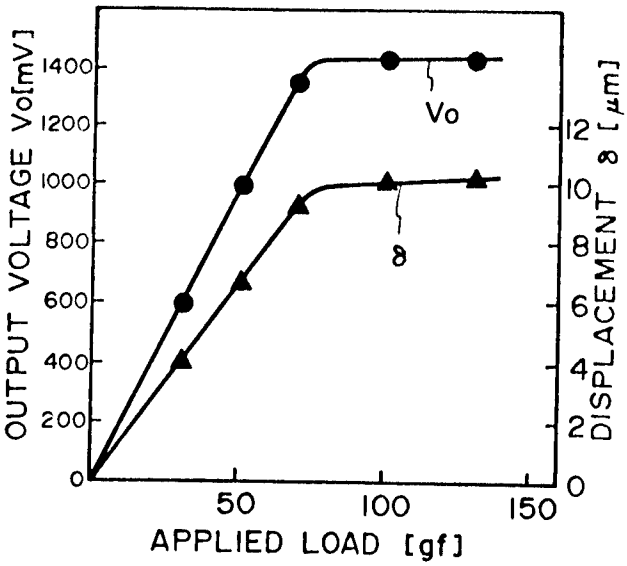


Fig.9. Measured transfer characteristics. Output voltage and displacement are shown in vertical axes.

spring constant without excessive warpage. The diffusion welding technology has been introduced to precisely join mechanical parts, such as a leaf-spring, in a micron order. Output voltage was 1360 mV and diaphragm center displacement was 9.2μm, respectively, for a 70 gf load. As the leaf-spring deflection is restricted on over 70 gf load, the silicon thin diaphragm could be protected against an overload. It is foreseen that a few gram maximum load would be measured with good linearity, by utilizing a thinner leaf-spring and thinner diaphragm.

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APPLICATION OF OPTICAL FIBER ARRAY TO CONTACT-TYPE IMAGE SENSORS

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ABSTRACT

To develope small-sized and high-fidelity input apparatuses for reading letters and images, we have studied the application of an optical fiber array for a novel optical system of compact contact-type image sensors instead of a lod lens array.

The illuminance on the photodetectors of 100 lx (570 nm yellow-green LED as a light source), the modulation transfer function (MTF) of 50% at 8 lp/mm of the image sensor and miniaturization of the sensor unit (e.g., a thickness of 6.4 mm) were attained. The illuminance obtained by the present optical system is about 4 times as large as that of the conventional one, and the resolution characteristics of the system are excellent as well.

A 2048 bits, 70 bits/mm linear charge coupled device (CCD) or a 1728 bits, 8 bits/mm a-Si:H thin film linear photodiode array is used as the photodetector of the image sensor. Letters(e.g., 8 point-size) and images of documents were read and reproduced by a thermal printer successfully.

1. INTRODUCTION

In recent years, contact-type image sensors have been developed for the use in facsimile apparatuses to miniaturze the apparatuses and reduce their production cost.[1-10] Most of the contact-type image sensors are generally designed so that information of documents reach the sensors through rod lens arrays. The document must be kept apart from the sensor by the total conjugate length of the rod lens array, so the thickness of a unit of the contact-type image sensor is 20∿30mm. Some of the contact-type image sensors[10] have no lens system, which results in a miniaturization of the apparatus. One of these image sensors is placed in direct contact with documents, which are irradiated through small windows fabricated on sensor substrates with light sources. Therefore the transmittance of light is low and it is difficult to keep the illuminance on the sensors high.

In contrast, the contact-type image sensors using optical fibers enable the unit to be miniaturized easily. But it is difficult to illuminate the document efficiently while maintaining the high resolution of the system. To overcome this problem we propose a new-type optical system with fiber arrays.

In this paper we report the characteristics of the new-type optical system and its application for a novel optical system of the contact-type image sensor.

2. PRINCIPLE OF OPTICAL SYSTEM

The optical fiber array consists of a great number of optical fibers whose diameter is about 25μm. These optical fiber arrays are generally classified between Clear-type and EMA(Extra Mural Absorption)-type according to the existence of light absorbing substance disposed between the adjacent optical fibers. The structures of Clear-type optical fiber array and EMA-type one are shown in Fig.1(a) and (b). In the Clear-type optical fiber array, light that is incident upon the optical fibers at angles of a certain value or more do not attain total reflection at the interface between the core and the clad, and the light reaches the adjacent optical fiber through the clad. Such leakage light reduces the quality of images. On the other hand, in the case of EMA-type optical fiber array, which is constituted by optical fibers with a light absorbing substance disposed between the adjacent optical fibers, the leakage light is absorbed and so the high resolution of the optical fiber array is maintained.

The MTF characteristics of the Clear-type optical fiber array and the EMA-type one are shown in Fig.2. The EMA-type optical fiber array has the MTF of about 80% at a spatial frequency of 4 lp/mm, that is clearly superior to that of the Clear-type one. However, when this EMA-type optical fiber array is applied to a contact-type image sensor, it is difficult to irradiate the document with a light source because of the light absorbing substances. If a certain gap is set up between the document and the optical fiber array so that a light can be introduced to the document, the resolution of the system is reduced.

The conbined optical fiber array (Hybrid-type optical fiber array) of Clear-type one and EMA-type one, shown in Fig.1(c), is proposed. This system enables the problem mentioned above to be

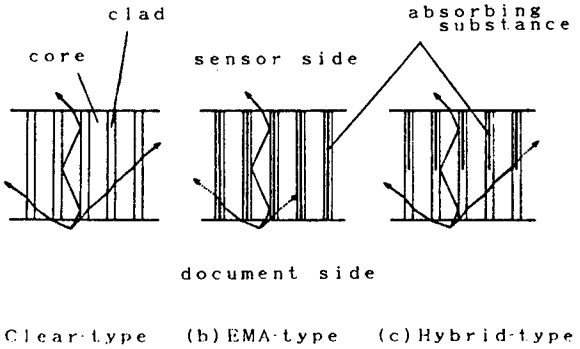

Fig.1. Structure of optical fiber array. (a)Clear-type, (b)EMA-type, (c)Hybrid-type optical fiber array.

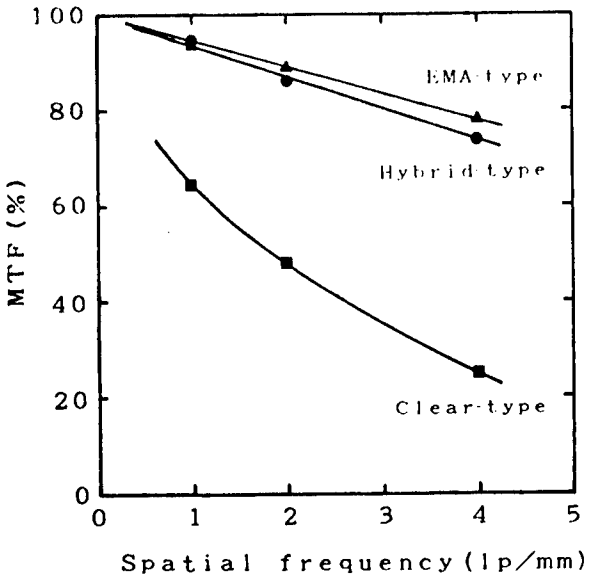

Fig.2. MTF characteristics of Clear-type, EMA-type and Hybrid-type optical fiber array.

settled. When this Hybrid-type optical fiber array is applied to a contact-type image sensor, the document can be illuminated through the part of the Clear-type optical fiber array and the leakage light can be absorbed by the light absorbing substance of the EMA-type optical fiber array. The MTF of the Hybrid-type optical fiber array is shown in Fig.2. The Hybrid-type optical fiber array exhibits excellent MTF characteristics that are about the same as those of the EMA-type one.

3. CHARACTERISTICS OF HYBRID-TYPE OPTICAL FIBER ARRAY

Figure 3 shows the dependence of the Hybrid-type's MTF upon the gap between the document and

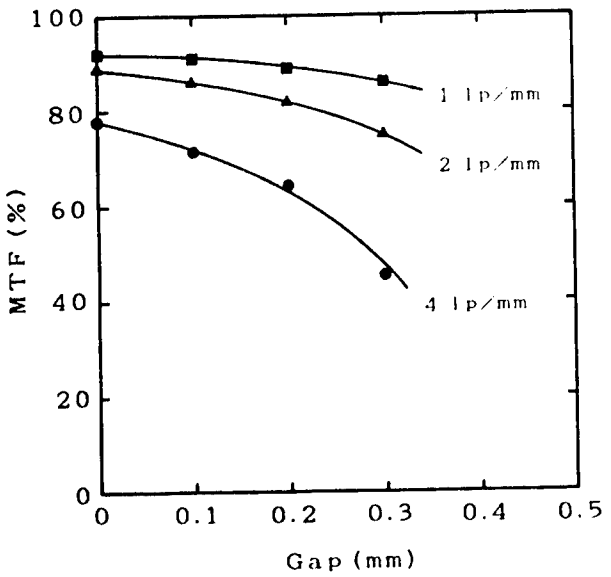

Fig.3. Dependence of the Hybrid-type's MTF upon the gap between a document and optical fiber array.

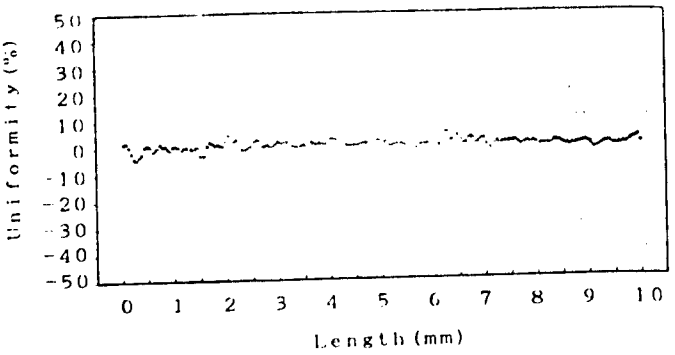

Fig.4. Measured uniformity of the transmittance of the Hybrid-type optical fiber array.

the optical fiber array. When the gap was set at 0.3mm, the MTF of 45% at a spatial frequency of 4 lp/mm was obtained. The depth of field is about the same as that of a rod lens array.

The measured uniformity of the transmittance of the Hybrid-type optical fiber array is shown in Fig.4. The non-uniformity was less than ±4.5% and the mean transmittance was about 25%. The transmittance is more than 10 times as excellent as those of a conventional spherical lens and a rod lens array.

The transmittance of a light going across the Clear-type optical fiber array is shown in Fig.5, where d is the distance on the document surface that a light goes across the Clear-type optical fiber array.

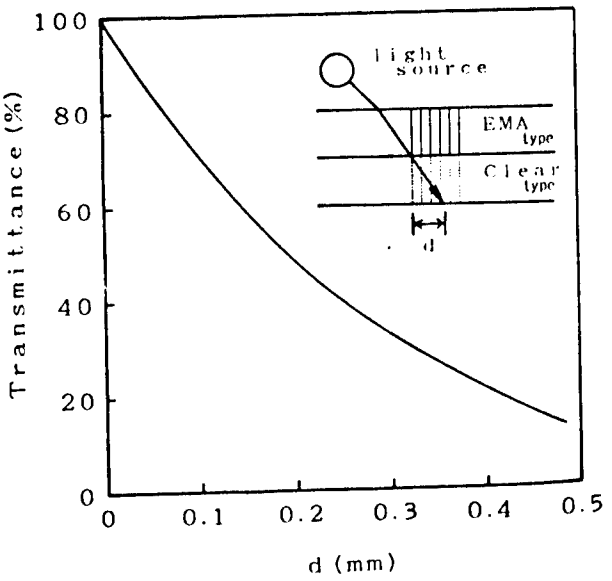

Fig.5. Transmittance of a light going across the Clear-type optical fiber array.

For example, the transmittance at the position of d=0.2mm is about 50%. In this case the total decaying rate of this optical system from the light source to the sensor is about 12.5%. Therefore, if the light source with the illuminance on the document of 800 lx is used, the illuminance on the sensor of 100 lx is attained. The illuminance obtained by the present optical

system is about 4 times as large as that of the conventional lod lens one.

Figure 6 shows the relation between the fiber diameter and the estimated MTF of the optical fiber array. The MTF is estimated by the number of the fibers occupying the corresponding area of each resolutions. When the fiber diameter is 25μm, the MTF is 50% at a spatial frequency of 8 lp/mm. It is reasonable to use the fiber whose diameter is about 25μm in case of application to contact-type image sensors with the resolution of 8 or 16 bits/mm.

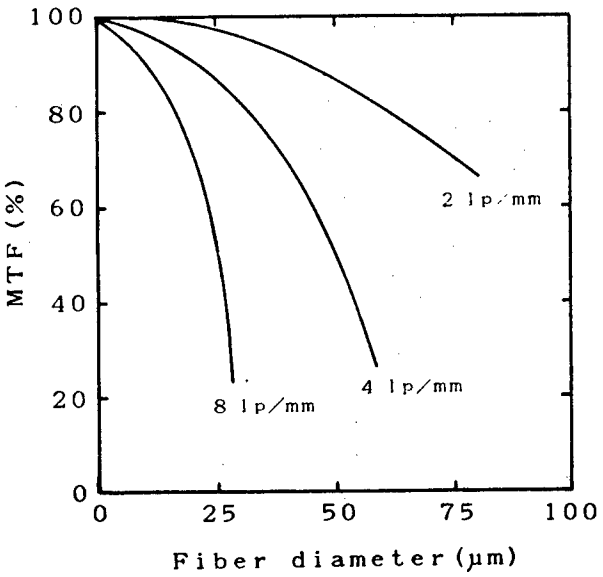

Fig.6. Relation between the fiber diameter and the estimated MTF of the optical fiber array.

4. APPLICATION TO CONTACT-TYPE IMAGE SENSORS

4.1 CCD IMAGE SENSOR

A cross-sectional view of the contact-type image sensor unit which consists of a Hybrid-type optical fiber array, a charge coupled device(CCD) and a light source is shown in Fig.7, where a 2048 bits, 70 bits/mm linear CCD is used. The sizes of the sensor unit are 19mm(W) × 7mm(D) × 50mm(L).

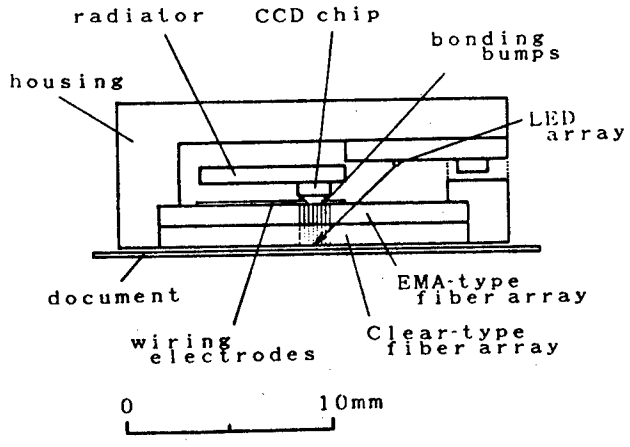

Fig.7. Cross-sectional view of the contact-type CCD image sensor unit which consists of a Hybrid-type optical fiber array, CCD sensor and a light source.

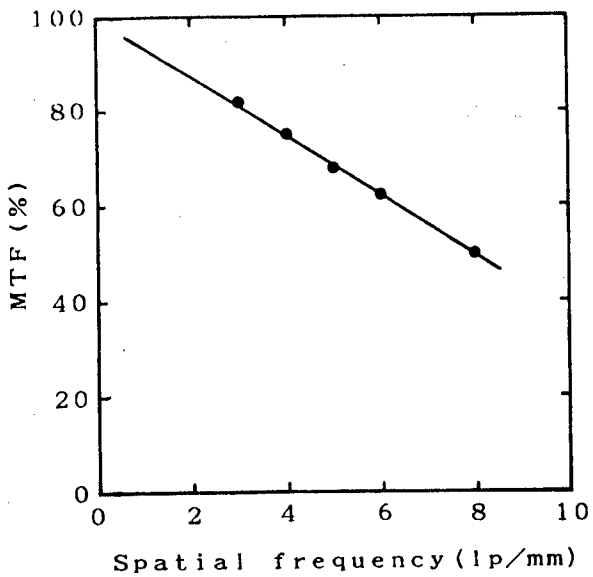

Fig.8. MTF of the contact-type CCD image sensor.

Electrodes on the CCD chip are bonded to wiring electrodes formed on the EMA-type optical fiber array by the use of bonding bumps. By the use of the 570nm yellow-green LED array without a rod lens, miniaturization of the sensor unit and uniformity of illuminance (about ±2%) on the document were attained.

The MTF of the present contact-type image sensor is shown in Fig.8. The MTF of 50% at 8lp/mm was attained, which is superior to that of conventional contact-type image sensors.

An example of read and reproduced images of 8 point-size letters is shown in Fig.9. The read images are of good quality.

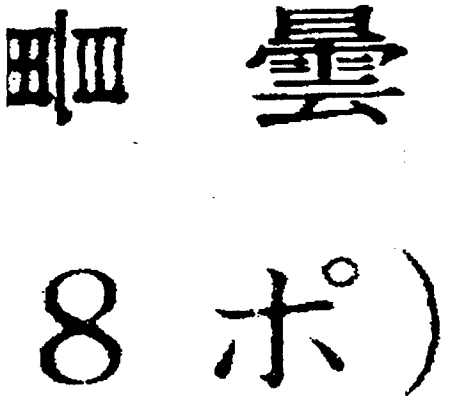

Fig.9. Example of read and reproduced images of 8 point-size letters.

4.2 a-Si:H IMAGE SENSOR

A cross-sectional view of the contact-type image sensor unit which consists of the Hybrid-type optical fiber array, an a-Si:H sensor and the

LED array is shown in Fig.10, where a 1728 bits, 8 bits/mm a-Si:H thin film linear photodetector array is used. The dimentions of the sensor are 32mm(W) × 6.4mm(D) × 254mm(L).

The signal waveform of a resolution test chart is shown in Fig.11. The MTF of 60% at 4 lp/mm was obtained. An example of reproduced images is shown in Fig.12. The reading of images was performed successfully.

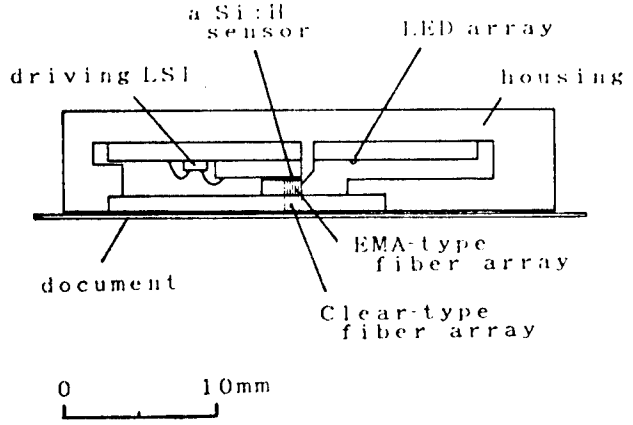

Fig.10. Cross-sectional view of the contact-type a-Si:H image sensor unit which consists of a Hybrid-type optical fiber array, an a-Si:H sensor and a light source.

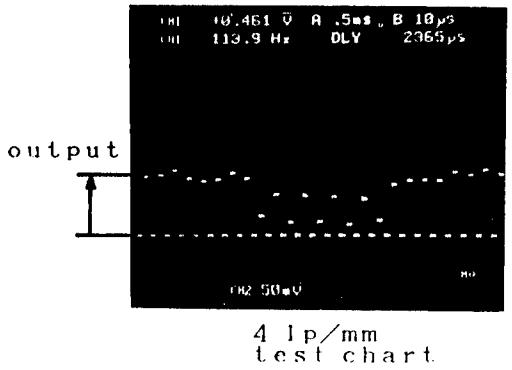

Fig.11. Signal waveform of a resolution test chart.

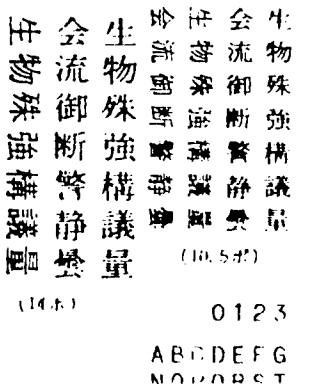

Fig.12. Example of reproduced images.

5. SUMMARY

The novel optical system composed of Clear-type optical fiber array and EMA-type one for contact-type image sensor has been developed instead of a conventional lens system such as a rod lens array.

The optical system exhibited the MTF of 50% at 8 lp/mm, about the same depth of field as that of a rod lens array, the uniformity of less than ±4.5% and the high transmittance of about 25%.

By the application of the present optical fiber array to contact-type image sensors, the high illuminance on the photodetectors, the high resolution characteristics and miniaturization of the sensor unit were attained and the readings of images were achieved successfully.

ACKNOWLEDGEMENTS

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TITANIUM NITRIDE-MOLYBDENUM METALLIZING METHOD FOR ALUMINUM NITRIDE

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Abstract

A paste containing molybdenum (Mo) and titanium nitride (TiN) powders was printed on aluminum nitride (AlN) substrates and was post fired. An adhesion strength of metallized substrates with Ni/Au plate was about 25kg/2.5mm$^{\square}$ and was unchanged after thermal cycle test. TiN-Mo does not adhere to the grain boundary phase in AlN substrate nor to surface oxide layer but to the AlN grain itself. This method, therefore, seems to be applicable to any kinds of AlN substrates, which may have different grain boundary oxide phases and thermal conductivities.

This TiN-Mo metallized AlN substrate was tried to displace a beryllium oxide (BeO) heat sink, which has been used for RF power transistors. There was no trouble in assembing the AlN heat sinks into transistors. Thermal resistance and electrical properties for transistors with AlN heat sinks were almost equal to those with BeO heat sinks. The TiN-Mo metallized AlN substrates were found to be able to replace BeO substrates as the heat sink for semiconductor devices.

1. Introduction

The AlN is well-known as a suitable material for high power device heat sinks or for IC ceramic packages, because of its high thermal conductivity and a thermal expansion coefficient close to that for silicon. A conductive layer on the AlN substrate is needed for these applications. A lot of metallization methods used for aluminum oxide (Al2O3) ceramics are applicable to AlN substrates in principle[1]-[5]. The purpose of this study is to establish a metallization method similer to the Molybdenum-Manganese (Mo-Mn) method for Al2O3 ceramics, for the mass production of heat sinks.

In the Mo-Mn method for Al2O3, metallization ingredients adhere to the grain boundary phases in Al2O3 substrates. As highly thermal conductive AlN substrates have few grain boundary phases, it is difficult to directly transfer the Mo-Mn method to AlN ceramics. A metallization method, in which metallization ingredients adhere directly to the AlN grain, is required.

Active metal brazing alloy, such as Ti-Ag-Cu, is used to adhere AlN ceramics to metal[3]. Titanium (Ti) is applicable to adhere AlN ceramics to metal directly. A high titanium-concentration reaction product, that forms at the metal-AlN interface, is TiN[6]. Though an active metal method is useful for causing AlN ceramics and metal to adhere, it is unsuitable for making up fine patterns on AlN substrates.

This study, therefore, has been undertaken to assist in developing a metallization method by printing, using TiN based powder. There are three important points which must be considered in order to develope strongly adhesive metallization substrates.

(1) The strength of the metallization layer itself.
(2) Strong adhesion between AlN substrates and metallization layer.
(3) There must be no damage to AlN substrates, such as residual stress and chemical reaction, which would weaken the substrates.

This study was made to foster matallization ingredients adhering directly with AlN grain, 260W/m·K-AlN substrates which had no grain boundary phase, were used. This is because AlN substrates usually contain a grain boundary phase, such as Y2O3, 2Y2O3·Al2O3, Y2O3·Al2O3, 3Y2O3·5Al2O3. Once a method for direct metallizing to AlN grain is successively developed, this method is thought to be applicable to any kinds of AlN ceramics. Finally, metallized AlN heat sinks were tried to displace BeO heat sinks, which have been used for RF power transistors, in order to find a possibility for replacing BeO heat sinks.

2. TiN-Mo metallization

2.1 Metallization method and adhesion test

AlN substrates, which had thermal conductivity of 260W/m·K with no grain boundary phase obtained from Toshiba R&D center, were used. The surface roughness (Rmax) for the substrates was 8μm and below. Average grain size for the substrates, measured by SEM observation, was in 10-15μm. Average powder sizes for Mo (Toshiba), TiN (Nihon Shinkinzoku) and Ti (Koujundo Kagaku) was 1.2, 0.8 and 7.5μm, respectively. Table 1 shows characteristics for these powders.

In order to investigate the possibility of other active metal compounds, TiN paste was prepared, in addition to Ti paste. 2.0mm square pads were printed out in 15μm sections on the 25.4x25.4mm AlN substrates. These samples were fired at 1873, 1973 and 2073K under a nitrogen atmospheric pressure. Then Ni (3-5μm) and

Table 1. Powder characteristics

Powder	Average grain size (μm)	Impurities (%)									
		Fe	Al	Ca	Mg	Ni	K	Cr	Zn	W	Co
Ti	7.5 [1]	0.02	0.01	0.001	0.01	0.01	—	0.008	0.001	—	—
TiN	0.85 [2]	0.11	5 *	5 *	—	0.005	—	0.01	—	1.7	0.1
Mo	1.2 [3]	0.003	5 *	—	5 *	0.02	5 *	—	—	—	—

1) Stokes' diameter
2) Permeametry (Fisher)
3) Permeametry (Blaine)
* (ppm)

Au (1-1.5μm) were plated, successively. 1.0mm diameter pins were 63Sn-Pb soldered on the 2.0mm□ pads. The adhesion strength was measured by pulling the pin perpendicularly (5mm/min cross head speed).

Delamination for Ti metallization was found after firing and average adhesion strength was less than 2kg/2mm□. No adhesion strength was less than 2kg/2mm□. No delamination for TiN metallization was found after firing and average adhesion strength was about 5kg/2mm□. When sintered substances (10x10x7mm) of AlN (containing 4wt.% of $3Y_2O_3 \cdot 5Al_2O_3$) and TiN were hot pressed to 2kg/cm² at 2073K, AlN and TiN also adhered to each other. TiN was chosen for the adhesion element to AlN in this metallization study. Though TiN was confirmed to be the best element to adhere to AlN directly, adhesion strength was only 5kg/2mm□ in metallization. Some other elements had to be added to TiN paste in order to improve the adhesion strength. Mo was selected for this purpose.

Six different volume ratio for TiN-Mo pastes were prepared. They were Mo only ("Mo"), 2Mo:1TiN ("21TiN"), 1Mo:1TiN ("11TiN"), 1Mo:2TiN ("12TiN"), 1Mo:3.8TiN ("14TiN"), and TiN only ("TiN") and were printed on AlN substrates. These samples were fired at 2013, 2073 and 2133K under the same conditions. Adhesion strength was measured by the pull off test and the knife scratch test.

(1) When "Mo" was used, average pull off strength was 0kg/2mm□ at every firing temperature (Fig. 1), because no sooner than a soldered pin was chucked, destruction between metallization layer and AlN substrates occured. Delamination between metallization layer and AlN substrate is shown in SEM photographs of cross sectional views (Fig. 2). These photographs also show that the metal layer was densified.

(2) When "TiN" was used, the average pull off strength was only 2kg/2mm□ at 2013K. When the firing temperature was risen to 2073K, the average pull off strength increased to 5.7kg/2mm□. The value was almost unchanged, when the firing temperature was risen to 2073K or over (Fig. 1). Destruction occured in the metallization layer (Fig. 3), as TiN metallization layer was very porous (Fig. 2). Moreover, metallization layer powdery broke easily at every firing temperature according to the knife scratch test (Table 2), because of low density of TiN metallization layer (Fig. 2). However, adhesion between TiN and AlN was found by the observation of the destroyed AlN surface after the pull off test. TiN existed on its surface and its surface changed from its original color (transparent white) to black.

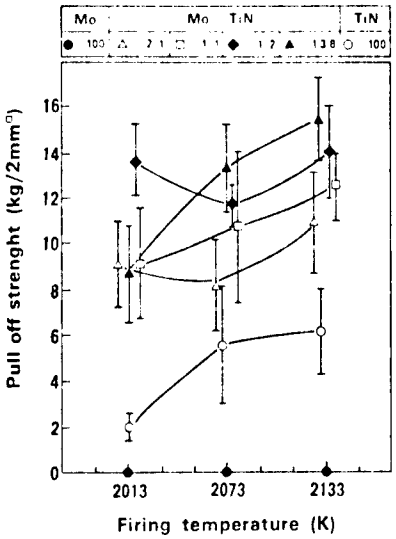

Fig. 1. Temperature dependency of pull strength of TiN-Mo pastes

(3) When TiN-Mo pastes were used, average pull off strengths were almost the same value on the whole, although the pull off strength for some TiN-Mo paste became higher for firing temperature rising (Fig. 1). The maximum pull off strength was much higher than that for only Mo and only TiN. Table 2 shows that TiN-Mo metallization layer broke in the layer itself at 2013K, in the knife test. When firing temperatures rose to 2073 and 2133K, "21TiN", "11TiN" and "12TiN metallization layers did not destruct. "14TiN" paste partly broke into powder. As TiN-Mo metallization layer was strong at 2073K, composition dependency of pull off strength was tested (Fig. 3). The combination of TiN and Mo raised the pull off strength more than only Mo or only TiN, although the metallization layer was rather porous (Fig.2). The average pull off strength became higher, as the amount of TiN increased (except 100vol.% TiN). The maximum adhesion strength was 13.4kg/2mm□ for "14TiN" paste. Destruction modes were different, i.e. "21TiN", "11TiN" and "12TiN" paste samples were destroyed in AlN substrates, while "14TiN" paste samples were destroyed in both AlN substrates and in metallization layer (Fig. 3).

Table 2. Destruction mode by knife scratch test

Paste \ Firing temp (K)	2013	2073	2113
Mo	C 1	C 1	C 1
2Mo : 1TiN	C 2	A 4	A 4
1Mo : 1TiN	C 2	A 4	A 4
1Mo : 2TiN	B 2	A 4	A 4
1Mo : 3.8TiN	C 2	A 3	A 3
TiN	C 2	C 2	C 2

A···strong. B···fairly strong. C···weak
1 ···delaminated between metallization layer and substrate
2 ···powdery destruction in the layer
3 ···partly powdery destruction in the layer
4 ···no destruction

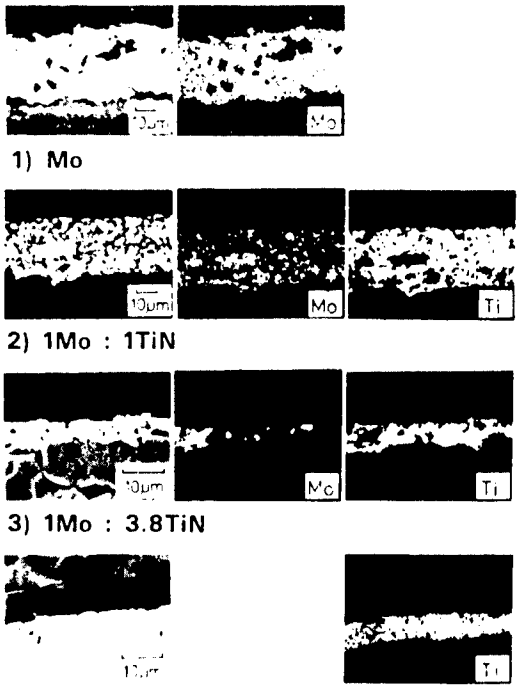

Fig. 2. SEM photographs of cross sectional view

The results indicated that TiN-Mo paste was the best for obtaining AlN metallized substrates.

2.2 Adhesion mechanism

When sintered AlN and TiN substances were hot pressed, they adhered to each other. When "TiN" paste was printed on AlN substrates and the samples were fired, AlN and TiN also adhered. The results clearly indicated that TiN was one of the essential substances to cause AlN ceramics to adhere in this TiN-Mo metallization method. However, the adhesion strength was only 5kg/2mm□ and was destroyed in metallization layer. Adding Mo to "TiN" paste resulted in adhesion strength being much improved, though "Mo" paste did not adhere to AlN. Destruction in AlN substrates was observed in TiN-Mo paste metallization substrates.

In order to consider the effects of Mo addition and the differences in destruction modes, shrinkage measurements for TiN-Mo mixed powders were carried out with cold pressed compacts. Five different volume ratio TiN-Mo powders were prepared, i.e. Mo only ("Mo"), 2Mo:1TiN ("21TiN"), 1Mo:1TiN ("11TiN"), 1Mo:2TiN ("12TiN") and TiN only ("TiN"). These compacts were fired at 1673, 1848, 1973 and 2123K under a nitrogen atmospheric pressure. Fired TiN-Mo compacts were determined by the X-ray diffraction method.

Three characteristics for TiN-Mo compacts were observed. First, the compacts kept their original shapes after sintering. Second, no TiN-Mo compound was detected. Mo did not react with TiN. Mo was partly changed into Mo2C. Third, regardless of the TiN contents, the surface of the compacts, including TiN, were all covered with TiN. TiN also covered Mo in metallization (Fig. 2). Moreover, when cold compacts of a mixture of AlN and TiN powder (weight ratio was AlN/TiN=1/4) were sintered, the compacts kept their original shapes and no TiN-AlN compound was detected. These result in no chemical reaction, which weaken AlN substrates in the metallization process.

This TiN-Mo metallization method was chemically stable. Physical conditions should be investigated. Temperature dependency of shrinkage for five kinds of metallization powder compacts is shown in Fig. 4. "Mo" compacts shrunk well. Even at 1673K, its shrinkage was 25.7% (relative density was 75%). On the contrary, "TiN" compacts and TiN-Mo mixed compacts shrunk gradually with temperature increasing. When Mo volume ratio in powder increased, final shrinkage became large. Mo was effective to shrink the compacts.

Cold compacts shrinkage properties explain different destruction modes in the pull off test. These results can be interpreted by residual stress in AlN substrates after metallizing. When pastes were printed on the substrates, it is rather difficult to shrink at freely like cold compacts. Consequently, the richer the Mo volume was, the more the compressive stress to the AlN substrates increased.

Though richer Mo weaken the AlN substrates strength by compressive stress, an appropriate quantity of Mo, i.e. 21 and 33 vol.% Mo, tightens the metallization layer itself and strengthens the mechanical adhesion strength, without damaging AlN substrates.

A fracture mode for "TiN" paste was in the metallization layer, near the boundary between substrates and metallization layer. Though little densification of "TiN" compact and powdery destruction in the knife scratch test indicate that "TiN" paste was not strong, the destruction did not occur on the metallization layer surface. This means that Ni plate reinforced the metallization layer.

3. Characteristics of metallized substrates

TiN-Mo adhered to AlN substrates with 260W/m·K thermal conductivity. Adhesion strength was also measured for the TiN-Mo metallized AlN substrates with thermal conductivities of 70, 130, 170 and 200W/m·K. These metallized substrates have different amounts of grain boundary oxide phases. Sample size was 2.5x2.5mm. 2.2mm diameter nail headed pins were used in the pull off test. Average strengths were 30.6kg, 24.2kg, 28.7kg and 26.5kg for the respective metallized substrates. Therefore, this TiN-Mo method was found to be applicable to AlN substrates for thermal conductivity 70-260W/m·K.

After thermal cycle test (TCT) (MIL-STD-883C-1010.2 condition D;-65℃(30min)-RT (5min)-200℃(30min) for 100 cycles), adhesion strength for samples which had 200W/m·K thermal conductivity was measured (Fig. 5). Adhesion strength after TCT maintained its initial value (25-27kg).

In addition to higher adhesion strength, metallized substrates require a smooth surface, high die bondability, strong wire bondability, low burr height, high electrical resistivity and high breakdown voltage. ble 2 shows the evaluation results for heat sinks.

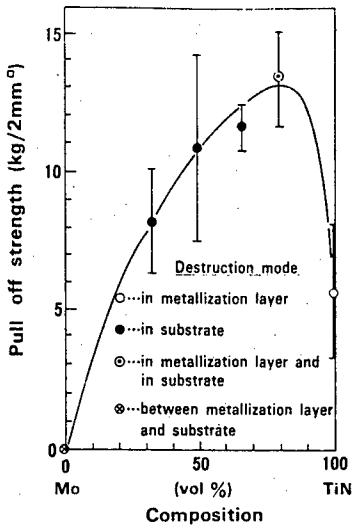

Fig. 3. Composition dependency of pull strength (at 2073K)

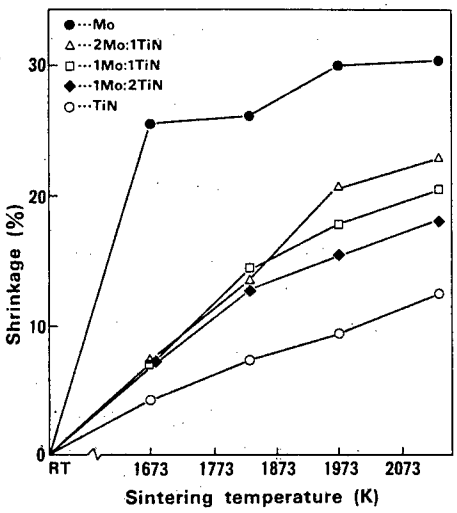

Fig. 4 Temperature dependency of shrinkage of TiN-Mo compacts

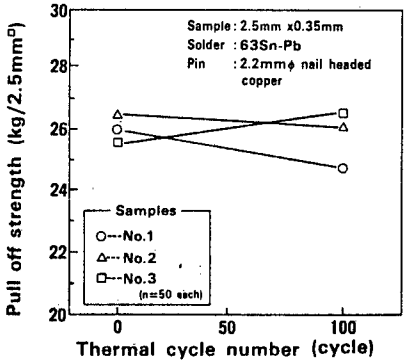

Fig. 5. Thermal cycle dependency of pull strength

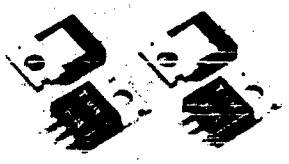

Fig. 6 RF power transistors

(1) Surface roughness (Rmax) was 6μm and below, while that for original substrates before metallization was 4-5μm.
(2) Semiconductor die bonding properties were examined, using 2mm x 2mm size samples. Silicon chips and substrates were scrubbed against each other. They were removed, while the solder was melting and were observed under 20x microscope. Au-Si and Au-Ge solders were used in a nitrogen atmosphere at 673K, and Sn-Sb and Sn-Pb solders were used in air at 503K. Excellent solderability was provided for all the solders. Adhesion strength between Ni plated layer and Au plated layer was strong enough to achieve wire bonding after being soldered.
(3) No blistering was observed when the substrates heated up to 673K.
(4) Wire pull off strength ranged from 20g to 30g, when aluminum wire (50μm) was bonded by ultrasonic (US) bonder.
(5) No burr height at the edges was observed under 20x microscope. The height was less than 2μm.
(6) Electrical resistivity was over 10^{14}Ω·cm.
(7) Breakdown voltage was over 14kV/mm (DC) for 1.5-7mm square metallized substrates.

Table 3. Metallized AlN substrate

Evaluation Item	Condition	Result
Surface roughness (μm)	——	Rmax 6μm (n=50)
Die bondability	Au/Si, Au/Ge 673K, N$_2$ Sn/Pb, Sb/Sn 503K, air	excellent
Blistering	673K, N$_2$, 10sec	not found
Wire bondability (g)	Al 50μm DIA, US bonder	20-30
Burr height (μm)	——	2μm (n=50)
Electrical resistivity (Ω·cm)	DC 100V	over 10^{14} (n=50)
Breakdown voltage (kV/mm)	DC	14-15 (n=15)

1) TiN-Mo metallization with Ni/Au plating
2) Thermal conductivity is 200 W/m·K

4. Application for RF power transistors

The AlN metallized substrates were applied to a heat sink for RF power transistors. Thermal conductivity for AlN substrates was 200W/m·K, while that for BeO was about 250W/m·K. The sample size was differently designed, between AlN and BeO, in order to make thermal dissipation close. The thickness of metallized AlN heat sinks was 0.35mm, while that for 99.5% BeO was 0.6mm. Molded final products for RF power transistors are shown in Fig. 6. Assembling transistors with AlN heat sinks was successfully carried out, as metallized AlN substrates had a smooth surface, an easily wettable surface with solders, a strong wire pull off strength and almost zero burr height, as previously described. Thermal resistance for both transistors was measured by ΔV_{BE} method. Figure 7 shows that transistors mounted on AlN heat sinks had slightly higher thermal resistance than those on BeO. It also shows the constancy of thermal resistance after TCT.

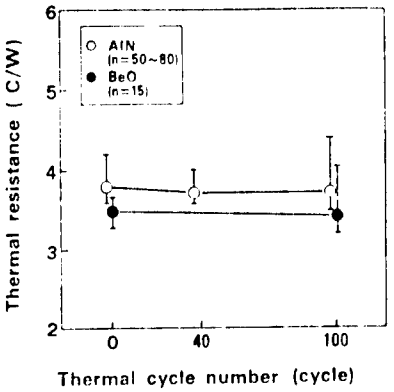

Fig. 7 Heat cycle dependency of thermal resistance of transistor

Load mismatch capability was measured by two tone (28.000MHz/28.001MHz) load pull test. That for the transistor mounted on AlN heat sinks was 19V, while that on BeO was 18V.

These results indicate that TiN-Mo metallized AlN heat sinks are able to replace BeO heat sinks.

5. Summary

(1) TiN-Mo adhered to AlN substrates (260W/m·K) with no grain boundary phases, by printing method. Its average adhesion strength was 13.4kg/2mm□.
(2) TiN adhered to AlN grain directly, although its metallization layer strength was weak. Mo improved the metallization layer strength and adhesion strength was also improved.
(3) As AlN, TiN and Mo did not react to one another, there was no chemical reaction which weakened AlN substrates in the metallization.
(4) Destruction in AlN substrates was caused by residual stress, which occured in AlN substrate, when Mo shrunk in the metallization layer.
(5) Ni/Au plating reinforced the metallization layer strength.
(6) TiN-Mo method was applicable to any kinds of AlN substrates, which had different grain boundary oxide phases and thermal conductivities. Adhesion strength was unchanged after thermal cycle test.
(7) AlN heat sinks had a smooth surface, an easily wettable surface, a strong wire pull off strength and almost zero burr height.
(8) Thermal resistance and load mismatch capability for a transistor with AlN heat sinks were close to the value for BeO heat sinks.
(9) TiN-Mo metallized AlN substrates were found to be able to repalce BeO substrates as the heat sinks for semiconductor devices.

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AUTOMATION OF LSI MANUFACTURING

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Automation of LSI manufacturing has been in progress, mainly for the purpose of its productivity increase, owing to the automation of an individual production equipment, the development and use of the production management system, and the intgreation of multiple equipments. Recently, big efforts are being made for realizing a totally automated manufacturing plant.

We also have been moving steadily ahead with the automation in LSI manufacturing, and we have obtained satisfactory results. More specifically, we achieved already a perfect automation for the production of DRAMs and ASICs.

In this paper, our automation of LSI manufacturing is introduced, picking up several aspects of the automation in our LSI manufacturing factories.

1. Introduction

1. 1 Features of LSI manufacturing

LSI manufacturing is roughly divided into the following three processes, as illustrated in Fig.1.

1) Wafer Fabrication

2) Assembly

3) Final Testing

In the wafer fabrication, circuits are formed on a silicon wafer through repetition of the mask-alignment and etching process, including oxidation, diffusion, chemical vapor deposition(CVD), ion implantation, and metallization, using a different mask for each process under super clean environment. In the assembly, many hundreds of LSIs on a silicon wafer are assembled to respective devices, by being cut, bonded, and molded. In the final testing, the devices are tested carefully before being shipped as the completed devices.

This LSI manufacturing has the following unique features which are unlike those in other industries:

1) The technology and products change very fast.

2) The production equipments are very unreliable, and the process capability is very low.

3) The investment in production equipments is huge and must be redeemed quickly.

4) The manufacturing line consists of wide variety of equipments supplied by wide variety of venders.

5) Super clean environment is needed

6) Especially in the wafer fabrication, the work passes many times through similer processes and through the similer or same equipments.

1. 2 Expected benefits by automation

Like other industries, automation of LSI manufacturing also has made progress, due to mainly its productivity increase under the circumstance where the markets needs for the products and their volumes vary very frequently. Automation of the manufacturing line is expected to provide the following several benefits:

1) The yield and quality of LSI chips become higher and stable because of eliminating human factors, namely, contamination from personnel, mis-operation due to human workers, etc.

2) The very complicated production management is simplified in the manufacturing line for large variety, small volume products like semi-custom ICs.

3) More precise control of the production equipments and the process conditions can be achieved by using, for example, feed back/feed forward system.

4) The lead time becomes shorter and the work-in-process decreases.

5) The number of workers is decreased.

2. Aspects of the automation in our LSI manufacturing line

We constructed already the totally automated lines for the production of DRAMs and ASICs. We have obtained satisfactory results in the automation. In this section, several aspects of the automation of the wafer fabrication in our line are described.

Fig.2 shows an example of a layout of our automated wafer fabrication line based on the open space clean-room. The open space clean-room is the clean-space structure in which equipments, work-in-process and personnel coexist. The transport system consists of automated guided vehicles (AGV) running on a "main street" at the center of the line, moving robots running in perpendicular to the "main street", and branch stations which transfer works between the AGV and the moving robot. A similar kind of equipments is gathered and placed along a route on which a moving robot runs, and the moving robot carries wafer cassetts between the branch station and loaders/unloaders of equipments. The branch station stores some amount of works for adjusting work-in-process or rearranges batches of works.

The production equipment, the AGV, and the moving robot in our line are given in more details below. In addition to them, IC card is also mentioned, which is applied for our line as the tool which helps the combination of an automated system and humans.

2.1 Equipment

Automation of equipment is attained, roughly speaking, by the automation of wafer-handling between equipment and transport, and by the automation of equipment control, as illustrated in Fig.3.

In the automation of wafer-handling, since most equipments for wafer fabrication have already been automated in the cassett-to-cassette manner and the cassette was standardized, no major problem exists. However, the manufacturing line consists of wide variety of equipments, so we drew up the specification of loader/unloader of equipment and standardized it in our line as the mechnical interface between transport and equipment.

The automation of equipment control is realized by providing each equipment with our original communication interface protocol between host computer and individual equipment, which was developed in accordance with SECS (Semiconductor Equipment Communication Standard). In accordance with our original protocol, the host computer gives the equipment such information as process recipes, remote start, and so on. Responding to the instruction of the host computer, the equipment sends the messages which mean process start, process end, and so on.

2.2 Automatic guided vehicle

The same kind of equipments is gathered and placed in the same fabrication area for the purpose of flexibility for change in variety and volume of products. The transport between these areas, generally, has a long and complicated route. So we newly developed the transport system which consists of automatic guided vehicles. This AGV can carry wafer cassetts in all direction guided by floor tape recognized by ITV.

This control system is illustrated in Fig.4. The AGVs are controlled by communicating to the traffic control CPU through communication loop and communication terminals which are equipped with each station of the AGV. The traffic control CPU puts information including source, destination, and its route (in terms of mark sequence recognized by ITV) for the AGV on the communication loop. The AGV receives instruction from the communication terminal and then moves to the destination taking the indicated path. The traffic control CPU is also controlled by host CPU. Therfore this transport system is included in the total automation system.

This transport system has the following features.

1) It is suitable for super clean environment (class 10)

2) Its AGV can move in all direction, which can save the space of the transport route.

3) It can operate for 24 hours without any interruption due to exchanging battery automatically.

4) Its AGV moves guided by floor tape recognized by ITV, therfore, it is easy to set up and relayout this system.

The AGV is shown in Fig.5 and its specifcations are indicated in Table 1.

2.3 Moving robot

The transport between equipments has a comparatively short and straight route, but it must load and unload a wafer cassette precisely and quickly. so we also newly developed the transport system which consists of moving robots. This robot is roughly divided into two section, manipulator and vehicle. Manipulator is a five axis horizontal joint robot, and vehicle has rail-guided structure and power is fed through cable.

This control system is illustrated in Fig.6. The traffic control CPU gives information about movements to the robot, in accordance with the instruction of the host CPU.

This transport system has the following features.

1) It is suitable for super clean environment (class 10).

2) Its robot performs precisely and quickly due to rail-guided structure and servo-control.

3) It has large service area (the maximum length of route : 20m, the maximum number of teaching points : 800 points).

The moving robot is shown in Fig.7 and its specifications are indicated in Table 2.

2.4 IC card

Since the ultimate purpose of automation is to make the production cost minimal, the total automation is not always the best solution, but the most appropriate combination of an automated system and humans sometimes more closely addresses this purpose. So we developed IC card applied for our line as a tool which helps the combination of an automated system and humans.
This IC card is attached to a wafer cassette and communicate with host computers through a communication terminal. The communication between this card and the communication terminal is implemented optically. This card can store some amount of data, and indicate some data from the stored data. By the indicated data, operators can get information such as lot number, next process, and so on.

3. Summary

We constructed fully automated LSI manufacturing lines by using the above mentioned production equipment, AGV, moving robot, and so on. We have obtained the following results by the automation.

1) Cleaness was extremely improved both locally and in the entire clean room.

2) The number of workers decreased to less than a half of that of our conventional line.

3) Defects on the wafer caused by manual handling were greatly eliminated.

4) Process data showed very tight distribution about the mean.

5) The number of lots rejected due to mis-operation by workers extremely decreased.

These results brought about the high and stable yield and quality of the products.

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Tab.1 Specifications of automatic guided vehicle (AGV)

Item	Specification
Payload	60kg
Speed forward lateral	0.6 m/s 0.25m/s
Acceleration	0.04G
Positioning repeatability	±5 mm
Guiding System	Tape recognition
Battery exchange interval(automatic)	8hours
Communication with external device	Laser communication
Steering	Four Wheel speed defferential
Safety device	Mechanical bumper Warnig chime
Physical dimention Weight	1200×750×580 mm 120 kg

Tab.2 Specifications of moving robot

Item	Specification
Dgree of freedom Manipulator vehicle	5 axis(01,02,03,04, Z) 1 axis(M)
Payload	3 kg
Speed 01 02 03 04 Z M	 90 120 177 100 300 mm/s 1 m/s
Positioning repeatability	±1 mm
Working envelope 01 02 03 04 Z M	 270 ±135 ±180 100 480 mm 2 m
Driving system	All electrical DC servo
Gripper control	Torque controlled
Safety device	Mechanical bumper Light beam switch

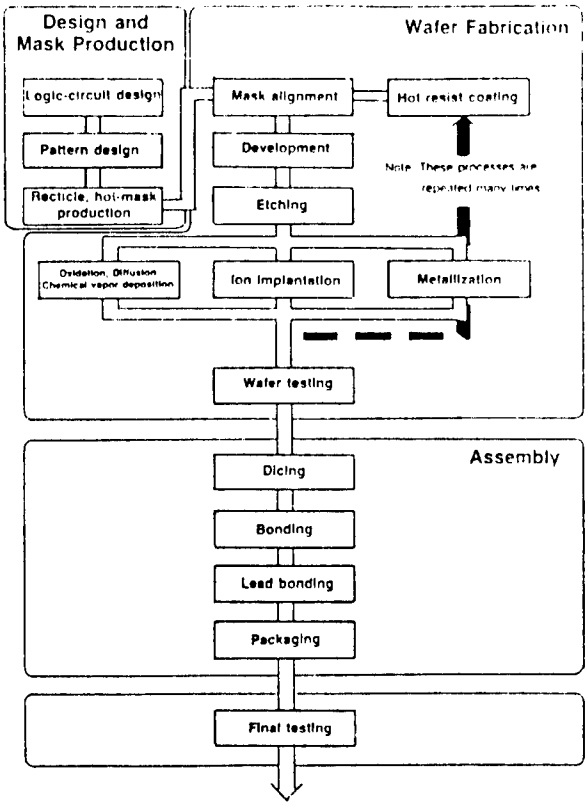

Fig.1 LSI manufacturing process

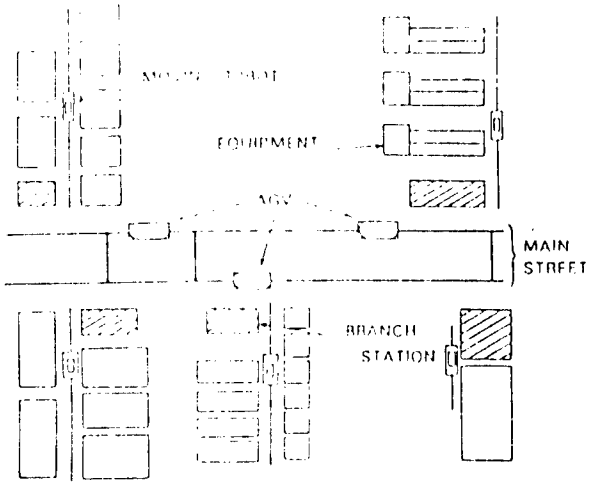

Fig.2 Example of layout of our automated wafer fab. line

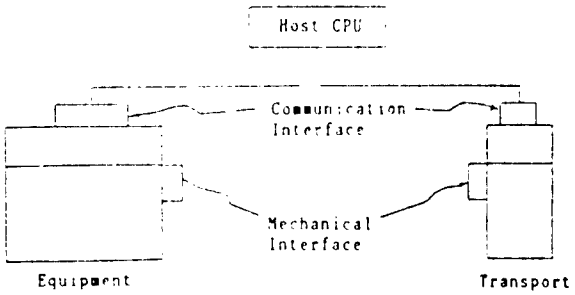

Fig.3 Automation of equipment

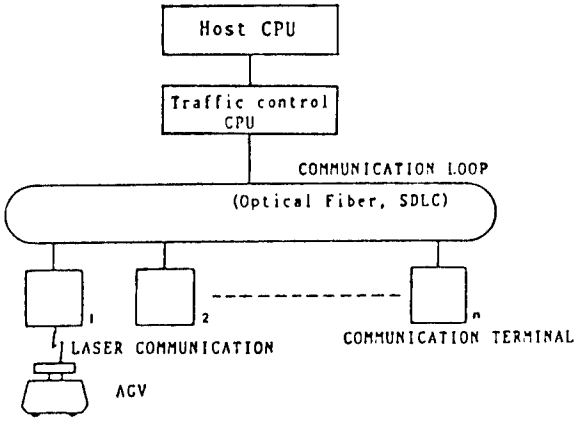

Fig.4 Automatic guided vehicle (AGV) control system

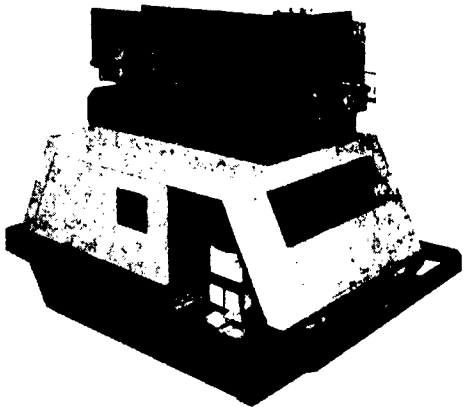

Fig.5 AGV

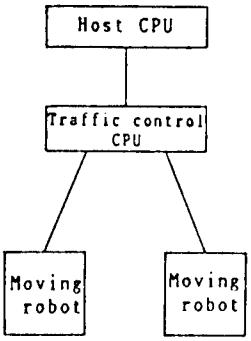

Fig.6 Moving robot control system

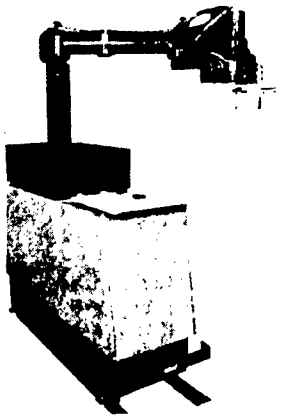

Fig.7 Moving robot

AN INTEGRATED INFORMATION SYSTEM FOR AN ELECTRONIC DEVICES PRODUCTION

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NEC Corporation

Accurate and speedy transfer of information is absolutely necessary if a business is to survive the intense competition of today's marketplace. Such needs can be met by a Computer Integrated Manufacturing System(CIMS) which augments human activities in all stages of production, from the receipt of an order through the designing and finally supplying the products.

We develop a comprehensive production information system called SFC (for Shop Floor Control). SFC is an important component of CIMS. SFC was developed to monitor and verify production information and to collect on a real-time basis such data as output volume, work-in-process, machine operating conditions, quality and costs.

1. INTRODUCTION

In today's cutthroat business market, it is strategically important for a company to accurately understand market needs and to make new and trendy products. The company's life depends on the quick response in developing and supplying products.

With this in mind, a comprehensive production information control system such as CIMS is clearly needed for speeding the flow of materials, products and information. We have technology centers in addition to system assembly plants and an electronic devices production factory. Each of these organization would like to speed up business decision-making, increase the effectiveness of management, respond quickly to changes and synchronize all production activities. The flow of products, materials andinformation, whether handled separately or as a unit, is expected to proceed quickly and reliably.

2. THE CONCEPT OF CIMS

2-1 Definition of CIMS

We define CIMS as "a comprehensive production system using the technologies of C&C (Computers and Communications) and FA (Factory Automation) to integrate all aspects of production management, from the receipt of an order to the design, manufacture and delivery of products.

2-2 Concept of the CIMS

We have three themes for realizing the CIMS:

(1) We must thoroughly rationalize the production system before the EDP approach. Automation does not equal rationalization. An EDP system alone cannot rationalize that which is irrational.

(2) Hierarchical division of functions
Company organization follows a hierarchical order. Responsibilities are distributed hierarchically due to individual limitations in the handling of data. The same applies to computer systems. Functions should be distributed hierarchically for simplicity. (Fig. 1) We consider three hierarchys; DIVISION CIMS, FACTORY CIMS, SFC.

(3) Loosely coupled integration
When systems are integrated but divided hierarchically, the systems must be interconnected through one simple interface. The goals are to avoid adverse effects on the system when accidents occur and to allow changes to be made easily as the system grows.

3. THE CONCEPT OF SFC

3-1 Definition of SFC

SFC is one element of the FACTORY CIMS. SFC controls various types of information in the production section, synchronizes materials and information and reduces the amount of indirect labor.

3-2 Basic model of SFC

Management of production lines is affected by many factors: differences of materials, assembly and handling, the physical construction of the lines, bottleneck points, the development of shop control over the years, and even the shop supervisor's personality, to name only a few. We have defined the following two basic models of SFC according to ideal methods of management and actual usage in other factories.

(1) RELATIONAL SFC
Product flow is influenced by relationships in the material tree structure. In every work center and production line, worker productivity is determined by the output of other lines. It is necessary to make precise scheduling in oder to synchronize the outputs of all work centers. This is the planning-type SFC. The system assembly plants are this type.

(2) NON-RELATIONAL SFC
Flow of products is simple and straitforward, because the structure of the material tree is also simple.

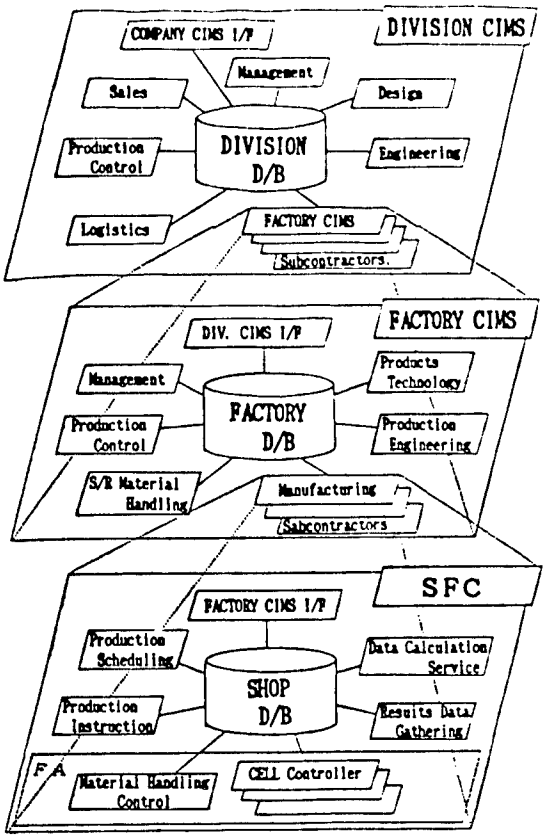

Fig. 1 Hierachcal Function Division

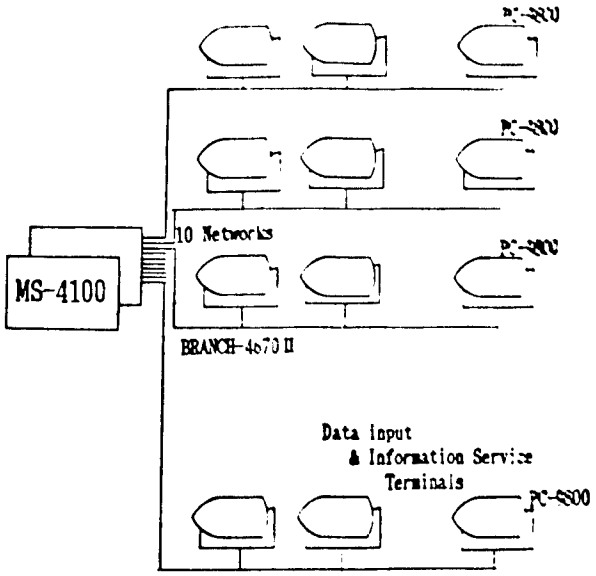

Fig. 2-1 System Configuration (Hardware)

The purpose of NON-RELATIONAL SFC is to maintain production volume with the maximum use of resources. In this case, it is most important to obtain accurate information about output, work-in-process, etc. This is an achievement-gathering type of SFC with real-time monitoring. The technology centers and the electronic devices production factories are this type.

These two basic patterns of SFC allow efficient development with applications for any system. I introduce the example of NON-RELATIONAL SFC.

4. THE BUILDING OF SFC IN DEVICES PRODUCTION TYPE LINES

4-1 Characteristics of the devices production type lines

In these production lines, the SFC system is the core of the FACTORY CIMS and is considered as a step toward a total CIMS. We have various production lines, each with a different method of assembly but with essentially the same type of management. The characteristics of the line are as follows:

(1) The structure of material tree and the production flow are simple.
(2) Production planning concentrates on input volume with regard to the workload.
(3) Production activities focus on the optimum use of resources (workers, machines, etc.) and elimination of defects.
(4) The key points of shop management are to accurately account for products and materials and to make sure that input materials are free of defects.

4-2 The concept of the NON-RELATIONAL SFC system development

It was developed with the concept that production information should be easily accessible "anytime and anywhere". The following three points are important for realizing this concept:

(1) Bar-code labels for easy inputting of data for synchronizing products and information.
(2) Use of network technology for on-line data processing in real time, all day long.
(3) The use of terminals for paperless management. (When we do use paper, it is done in a constructive manner.)

4-3 System configuration (Fig. 2)

4-4 Main functions

(1) Data input for workers
Every worker records the quantitiy (including defects) at every work center at the beginning and at the end of each job. (Fig. 3)
Every worker records the work time just before going home.
(2) Collecting data automatically
Data for machine operating conditions and stop items can be gathered automatically.

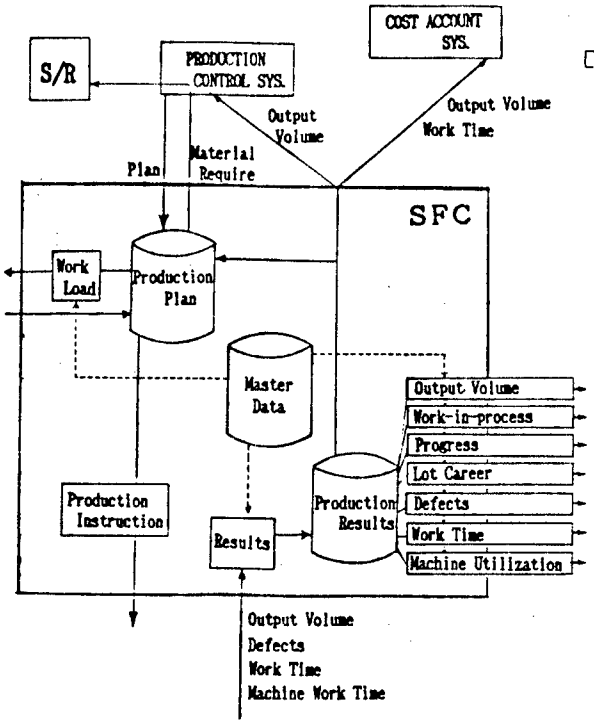

Fig. 2-2 System Configurateion (Function)

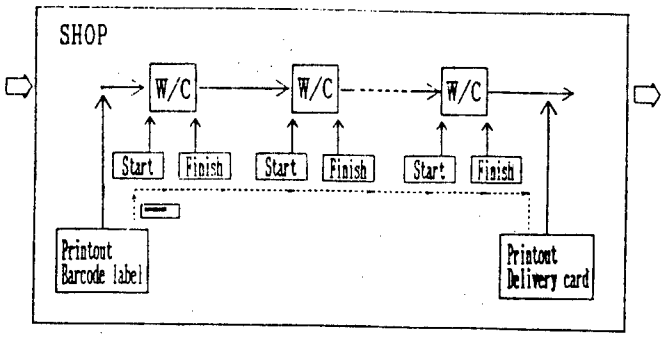

Fig. 3-1 Input Data Points

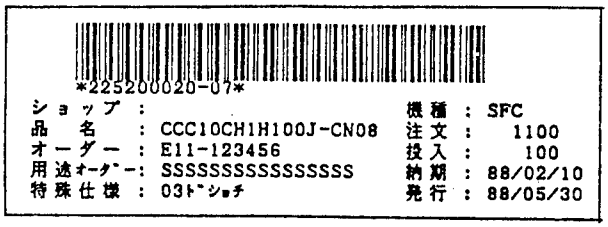

Fig. 3-2 Barcode Label Sample

(3) Out put volume reports (Fig. 4)
This is an input/output curve, which shows the defference between the plan and the actual results.
(4) Defect reports (Fig. 5)
The P-chart and Pareto chart are used for identifying problems.
(5) Word-in-process reports (Fig. 6)
Work-in-process information for every work center can be obtained promptly. The data can be used for job planning at the next work center.
(6) Progress reports (Fig. 7)
The progress of an order can be monitored. Such data can be used to predict the delivery date.
(7) Machine operating condition reports (Fig. 8)
Machine operating conditions and accidental stop items can be observed. This provides for prevention of product defect and better utilization of machines.
(8) Work load reports (Fig. 9)
Work load data can be observed.

4-4 Effects

The effects of the SFC system are as follows:
(1) Real-time production information can be obtained quickly, so that forecasts can be made more accurate.
(2) Problems and points of improvement for each work center are made clearer.
(3) Evaluation of alternatives is easier. Feedback response is quicker.
(4) Many kinds of report papers are generated automatically, which can save much time.

All this results in more aggressive improvement activities for the workers. Other good effects include quality improvement, reduction of lead time, inventory savings and better utilization.

5. Future CIMS

NON-RELATIONAL SFC has already been developed. I have some suggestions for building a CIMS for the development of manufacturing and management.
(1) Optimization of work-sharing by humans and computers. Humans and computers each have their own strengths and weaknesses. Human intelligence can not be developed if it relies too heavily on computers.
(2) Qualitative data must be converted to quantitative data carefully and thoughtfully if it is to be processed by computer. Otherwise, the vast amount of data that would be would require a large computer to process it.
(3) Optimum data should be provided for decision making. It is important to select only the necessary data.

Although CIMS means computer integration, its success depends on its use by everyone in the company. What do humans find confusing? What kind of work does the computer do best? What satisfies everyone, both workers and managers? The sensibilities of systems engineers should have a greater part in the building of CIMS. That is, CIMS of humans, by humans, and for humans.

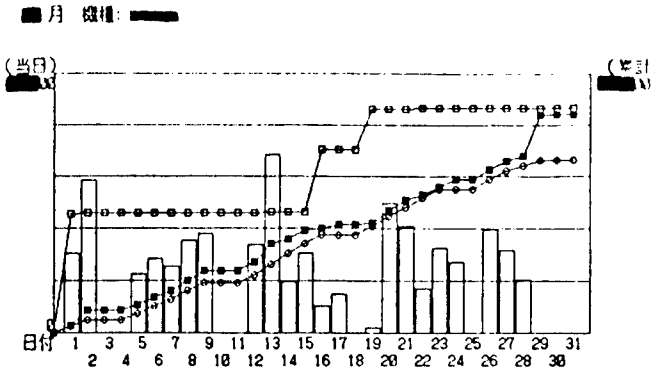

Fig. 4 Output Volume Reports
(Input/Output Curve)

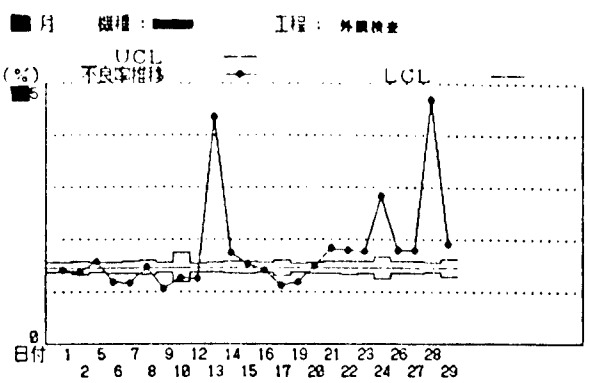

Fig. 5-2 Defects Reports
(P-Chart)

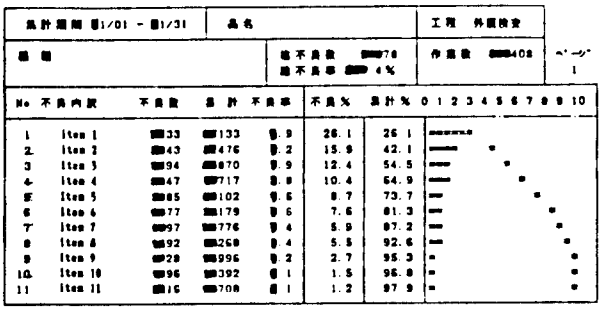

Fig. 5-1 Defects Reports
(Parete-Chart)

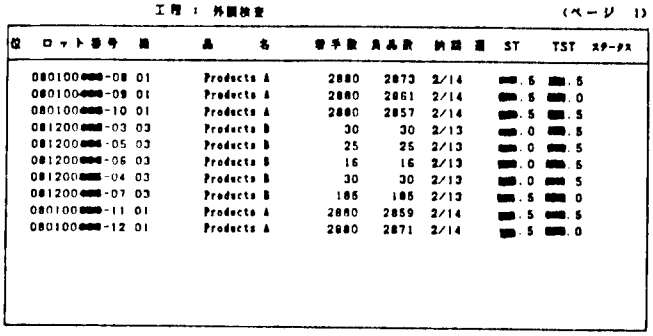

Fig. 6 Work-in-process Reports

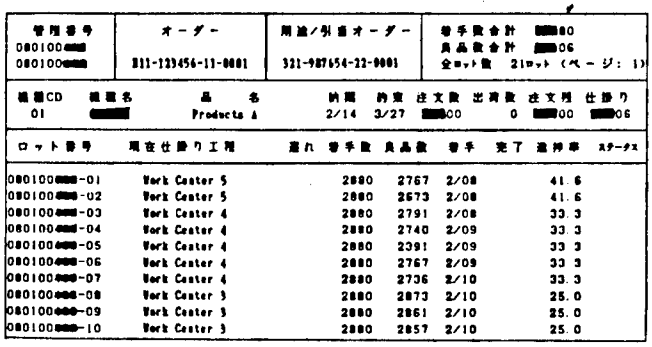

Fig. 7 Progress Reports

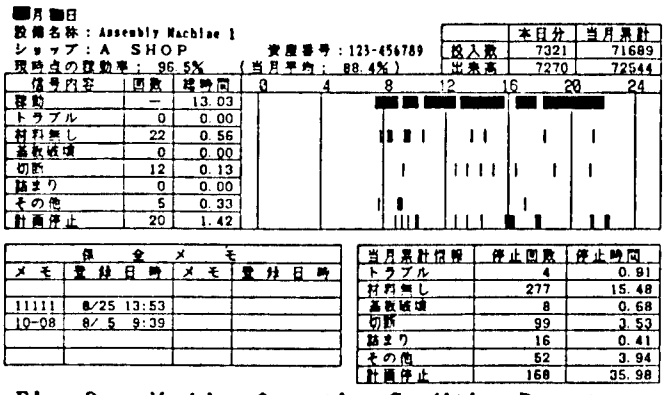

Fig. 8-2 Machine Operating Condition Reports
(Accidental Stop Items)

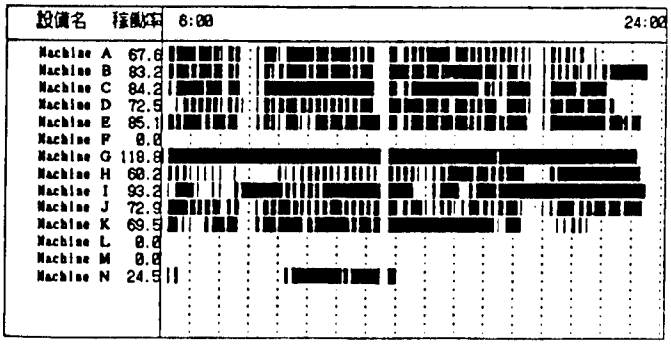

Fig. 8-1 Machine Operating Condition Reports
(Gant-Chart)

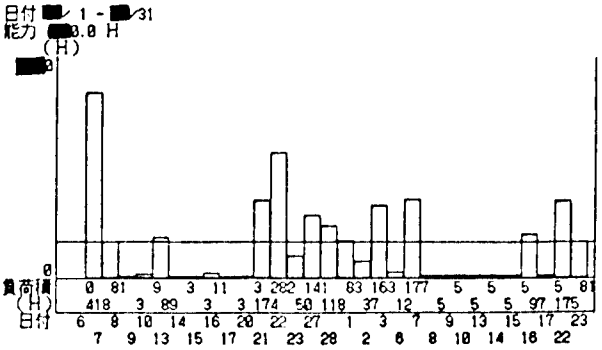

Fig. 9 Work load Reports

VARIATION OF ACOUSTIC IMPEDANCE CAUSED BY A CUT IN ULTRASONIC TRANSDUCERS

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Abstract

This paper describes our measurement of the acoustic impedance of the ultrasonic array transducer's backing.

The ultrasonic transducer consists of piezoelectric ceramic and backing and matching layers. An array transducer is made by sawing the piezoelectric ceramic into array elements.

The backing is also cut slightly so each element can be driven independently, without acoustic cross-coupling between elements. It was difficult to measure the acoustic impedance of the sawed part of the backing because it is very small.

We devised a way to measure the acoustic impedance of the sawed part of the backing. The method uses the reflection coefficient spectrum at the surface of the sawed backing. The measured impedance of the sawed part was 5.33×10^6 kg/m^{2}s and that of the solid part was 6.35×10^6 kg/m^{2}s. We clarified that the impedance of the sawed part of the backing is less than that of the solid backing, even though the material is the same.

From this, we were able to calculate the array transducer's electro-acoustic conversion characteristics with computer simulation accounting for the effect of the sawed part of the backing.

1. Introduction

Array transducers used in ultrasonic imaging for medical diagnosis usually have many independent elements. By driving each element with a delay, the beam can be made to produce a sector or a linear scan and focus at a predetermined distance.

An array transducer is made by forming a highly attenuative backing on one side of a piezoelectric ceramic substrate, plating a matching layer on the other side and sawing the ceramic substrate into array elements. The backing is also cut slightly (Fig. 1) so each element can be driven independently, without acoustic cross-coupling between elements[1].

It is necessary to know the acoustic impedance of the material the transducer is made of because the electro-acoustic conversion characteristics of the transducer depend on the impedance. Acoustic impedance is the product of density and acoustic velocity. Generally the acoustic velocity of an object depends on its shape, so we guessed that the velocity and the impedance of the sawed part of the backing was different from that of the solid part. The velocity of the solid part of the backing can be obtained easily because it is large, but it is difficult to obtain the velocity of the sawed part because of its minute form.

In this paper, we discuss how we measured the acoustic velocity and impedance of the sawed part of the backing and our results. We obtained the excellent agreement between experiment and simulation of the electro-acoustic conversion characteristics of the array transducer by considering the impedance of the sawed part of the backing.

2. Impedance of backing

Acoustic impedance Z is the product of density ρ and acoustic velocity c. Density ρ is the ratio of mass to volume, so acoustic impedance Z can be calculated from acoustic velocity c. Generally the velocity c of an object more than several millimeters thick, like the solid part of the backing, is calculated from the ultrasonic echo delay Δt and its thickness d (Fig. 2a) using

$$c = 2d/\Delta t \qquad (1)$$

However, for objects thinner than one millimeter like the sawed part of the backing, it is difficult to obtain its velocity from the ultrasonic echo delay because of their overlapping (Fig. 2b).

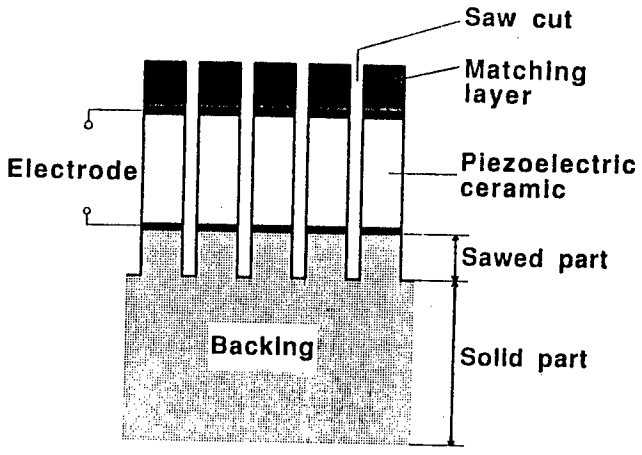
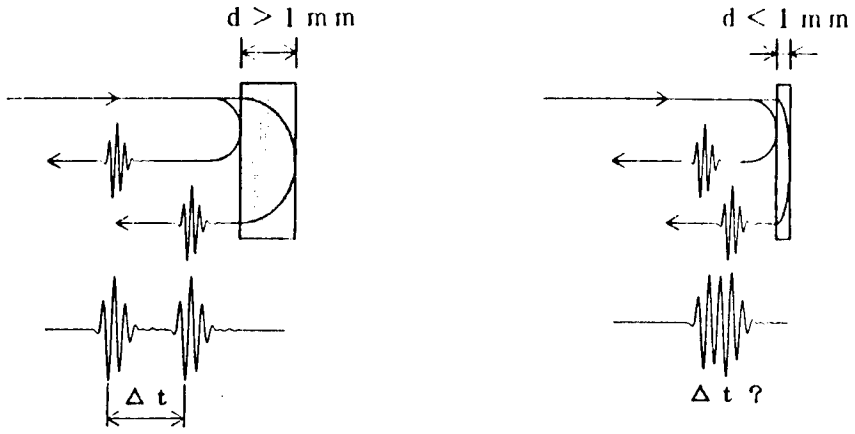


Fig. 1 Array transducer



(a) Thick object (b) Thin object

Fig. 2 Measuring velocity

We devised a way to measure the acoustic velocity of a thin object.

For a layer S between two acoustic media A and B (Fig. 3), the relation between the force F and the displacement velocity u in each medium is given by the transmission line equation

$$\begin{bmatrix} F_a \\ u_a \end{bmatrix} = \begin{bmatrix} \cos(\gamma d) & j Zs \sin(\gamma d) \\ \frac{j}{Zs} \sin(\gamma d) & \cos(\gamma d) \end{bmatrix} \begin{bmatrix} F_b \\ u_b \end{bmatrix} \tag{2}$$

and

$$\gamma = 2\pi f/c \tag{3}$$

where

F_a = force in the medium A
F_b = force in the medium B
u_a = displacement velocity in the medium A
u_b = displacement velocity in the medium B
Zs = impedance of the layer S
d = thicness of the layer S
c = acoustic velocity of the layer S
f = frequency

The acoustic impedance Zb of the medium B is given by

$$Zb = \frac{F_b}{u_b} \tag{4}$$

So from Eq. (2) and Eq. (4) the acoustic impedance Zb' of the medium A to the medium B through the layer S is given by

$$Zb' = \frac{F_a}{u_a} = Zs \frac{Zb \cos(\gamma d) + j\, Zs \sin(\gamma d)}{Zs \cos(\gamma d) + j\, Zb \sin(\gamma d)}$$

$$= \frac{1 + m\, e^{-j2\gamma d}}{1 - m\, e^{-j2\gamma d}} \tag{5}$$

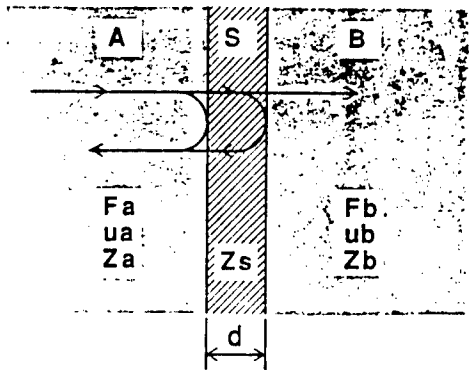


Fig. 3 A layer between two acoustic media

where

$$m = \frac{Zb - Zs}{Zb + Zs} \tag{6}$$

The reflection coefficient Γ at the interface of the medium A and the layer S is given by

$$\Gamma = \frac{Zb' - Za}{Zb' + Za} \tag{7}$$

so from Eq. (5), we get

$$\Gamma = \frac{(Zs - Za) + m(Zs + Za)e^{-j2\gamma d}}{(Zs + Za) + m(Zs - Za)e^{-j2\gamma d}}$$

$$= \frac{m' + m\, e^{-j2\gamma d}}{1 + mm'\, e^{-j2\gamma d}} \tag{8}$$

where

$$m' = \frac{Zs - Za}{Zs + Za} \tag{9}$$

Therefore, the absolute value of the reflection coefficient $|\Gamma|$ is given by

$$|\Gamma| = \sqrt{\frac{(m^2+m'^2) + 2mm' \cos(2\gamma d)}{(1+m^2m'^2) + 2mm' \cos(2\gamma d)}} \tag{10}$$

The reflection coefficient $|\Gamma|$ is periodic and has a maximum or minimum at

$$\gamma = \frac{n\pi}{2d} \qquad n = \text{integer} \tag{11}$$

as shown in Table 1.

Table 1 Reflection coefficient

$mm'>0$ ($Zs>Za$ and $Zb>Zs$ $Zs<Za$ and $Zb<Zs$)	$\lvert\Gamma\rvert_{max} = \left\lvert \frac{m+m'}{1+mm'} \right\rvert$	at $\gamma = \frac{2k\pi}{2d}$
	$\lvert\Gamma\rvert_{min} = \left\lvert \frac{m-m'}{1-mm'} \right\rvert$	at $\gamma = \frac{(2k-1)\pi}{2d}$ (k = integer)
$mm'<0$ ($Zs<Za$ and $Zb>Zs$ $Zs>Za$ and $Zb<Zs$)	$\lvert\Gamma\rvert_{max} = \left\lvert \frac{m-m'}{1-mm'} \right\rvert$	at $\gamma = \frac{2k\pi}{2d}$
	$\lvert\Gamma\rvert_{min} = \left\lvert \frac{m+m'}{1+mm'} \right\rvert$	at $\gamma = \frac{(2k-1)\pi}{2d}$ (k = integer)

Then if we define $\Delta\gamma$ between γ at which the reflection coefficient $|\Gamma|$ is at a maximum or minimum, we get

$$\Delta\gamma = \pi/d \tag{12}$$

Similarly, using frequency interval Δf, from Eq. (3) we get

$$\Delta\gamma = 2\pi\Delta f/c \tag{13}$$

Then from Eq. (12) and Eq. (13), we get

$$c = 2d\Delta f \tag{14}$$

Therefore, acoustic velocity c of the layer S is obtainable from the frequency interval Δf and the thickness d of the layer.

To obtain the velocity of the sawed part of the backing, we made some samples of it on stainless steel (Fig. 4) and observed its ultrasonic echo spectrum with the measurement setup in Fig. 5. The echo spectrum had many dips with a constant frequency interval Δf because of the reflection coefficient at the surface of the sample given by Eq. (9). We measured the frequency interval Δf at several thicknesses d, and calculated the velocity c of the sample with Eq. (14). The measured velocity for each thickness is shown in Fig. 6. The velocity is nearly constant between 0.1 mm to 0.6 mm at 2370 m/s. The velocity of the solid backing was obtained by conventional techniques. It was 2690 m/s. Table 2 shows the acoustic impedance of each part of the backing as calculated with its density ρ and velocity c.

The results show that the impedance of the sawed part is less than that of the solid backing because of the sawed part's decreased acoustic velocity.

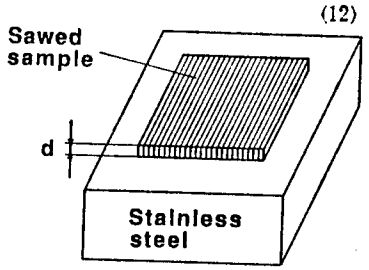


Fig. 4 Sample for sawed part of backing

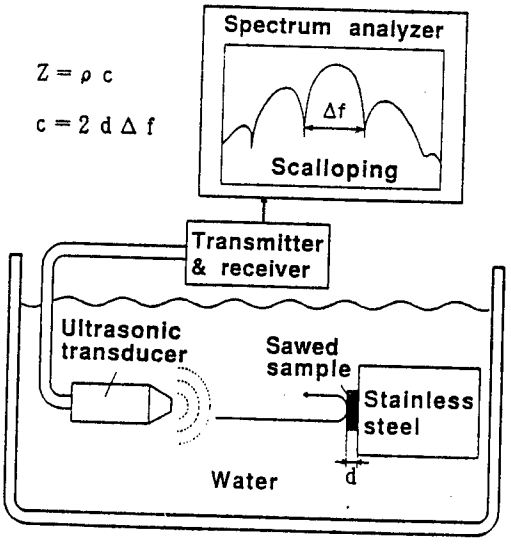


Fig. 5 System for measuring velocity

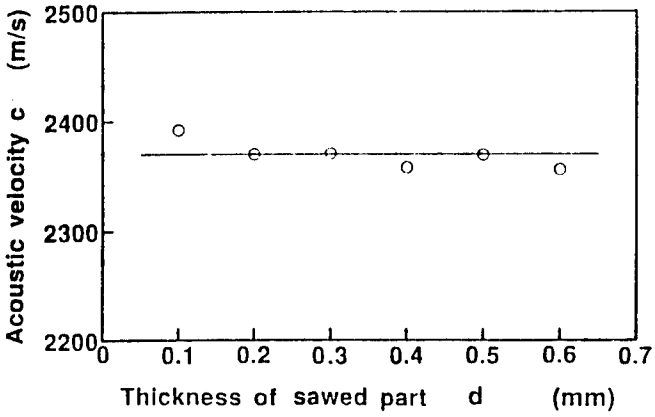


Fig. 6 Velocity of sawed part of backing

Table 2 Impedance of backing

Backing Sample	Density ($\times 10^3$ kg/m^3)	Velocity (m/s)	Impedance ($\times 10^6$ kg/m^{2}s)
Solid	2.36	2690	6.35
Sawed	2.36	2370	5.33

3. Characteristics of array transducer

From these results, we conclude that the sawed part of the backing acts as a pseudolayer between the piezoelectric ceramic and the backing in an array transducer (Fig. 7) because its impedance is lower than that of the backing.

To confirm this, we compared a simulation and an experiment of the array transducer's electro-acoustic conversion characteristics[2]. The simulated two-way gain spectrum accounting for the effect of the sawed part of the backing (the solid line in Fig. 8) is in excellent agreement with the measured two-way gain spectrum (the circles).

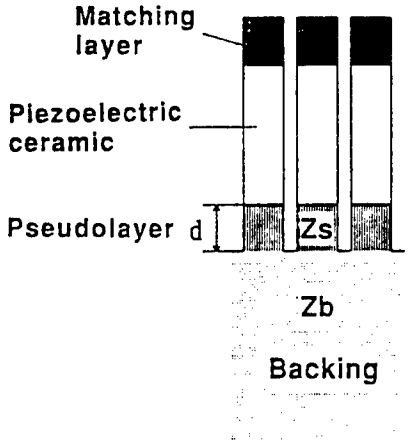


Fig. 7 Pseudolayer

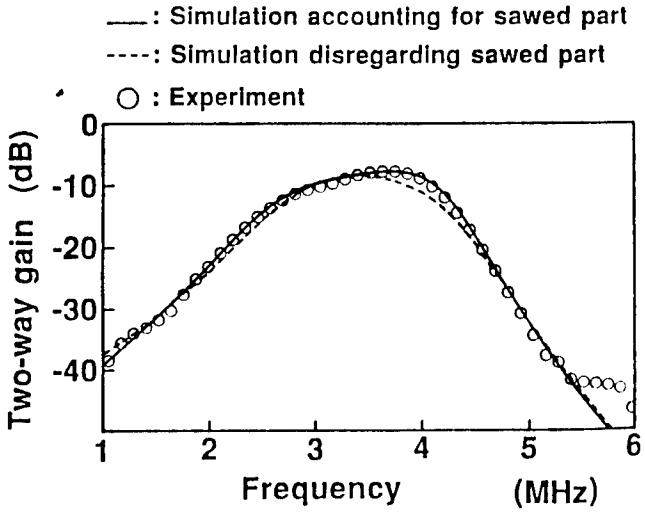


Fig. 8 Simulated and measured two-way spectra

4. Conclusion

We devised a way to measure acoustic impedance of a minute object and measured that of the sawed part of the backing in an array transducer. We clarified that the impedance of the sawed part of the backing is less than that of the solid backing, even though they are made of the same material. Our simulation of electro-acoustic conversion characteristics was in excellent agreement with experiment.

7. References

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ANALYSIS OF HIGH-SPEED BUS LINES IN PRINTED CIRCUIT BOARDS

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ABSTRACT

Techniques are investigated for improving the operating speed and driving capabilities of bus lines in a bookshelf-type packaging system. In particular, a parallel distributed circuit model with stubs is introduced for analyzing reflection and crosstalk noise simultaneously. Numerical analysis shows that a trade-off exists between the upper limit of speed and the number of packages, and that the reduction of stub length will improve the trade-off. Experiments indicate that reduction of stub length by surface mount bus drivers on both surfaces of a package is highly effective for achieving high operating speeds.

INTRODUCTION

Recent advances in VLSI technology have brought about changes in printed circuit board design. The number of SSIs (Small Scale Integration) mounted on a board has become lower and lower since most logic functions are now integrated in a few VLSIs. The remaining SSIs are receivers, drivers and transceivers only due to the fact that VLSIs themselves do not have sufficient driving capabilities. VLSIs, however, require wide-bit bus lines to communicate with each other[1]. For a large scale system, bookshelf-type packaging as shown in Fig.1 is widely used. The packaging system is constructed by connecting multiple packages to a backplane. As a result, bus lines have many stubs and long parallel lines which can cause serious multi-reflection and crosstalk noise. However, few papers describe how to control the transmission properties of bus lines. This paper presents techniques for improving the operating frequency.

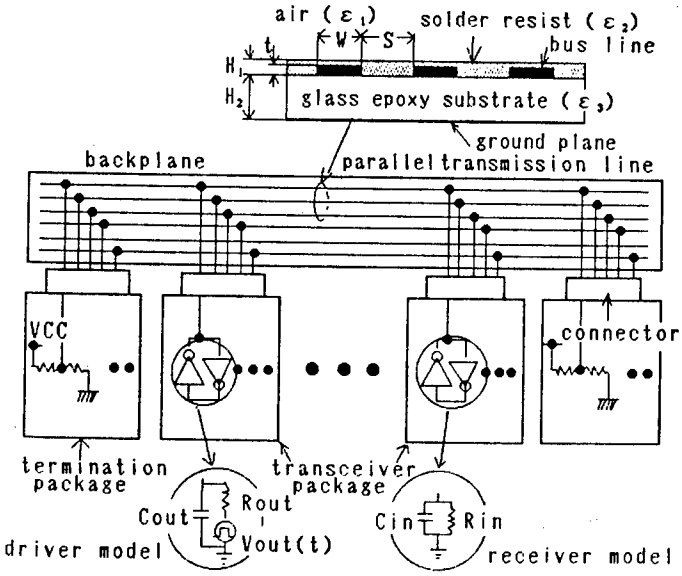


Fig.1 Bus line model.

ANALYSIS MODEL

Figure 1 shows the bus line model to be analyzed. Multiple packages are plugged into a backplane with connectors. The bus lines run parallel to each other and have many stubs. All stub lines on the packages are terminated by TTL transceivers which act as a driver or receiver. Both sides of packages mount terminating resistors.

The stub lines cause multiple reflection noise on the main routes since the impedance of stubs which act somewhat as open transmission lines is different from that of the main routes. In addition, the main routes, stub lines and connector pins construct parallel lines and induce a great deal of crosstalk noise as shown

Table 1 Line and device parameters used in the analysis.

(All line parameters are modified by the coupling between 1st and 3rd lines.)

Package & Backplane			
W	150 μm	ε_2	3.5
S	1120 μm	ε_3	5
t	18 μm	Ls	580nH/m
H_1	25 μm	Lm	1.6nH/m
H_2	200 μm	Cs	95pF/m
ε_1	1	Cm	0.27pF/m
Transceiver			
Tr	5.9ns	R_{OUT}	31Ω
Tf	2.8ns	C_{OUT}	15pF
Cin	15pF	Rin	10kΩ
Package spacing			
l	15mm		

in Fig.2. Therefore, to analyze the transmission line properties of a bus line system accurately, it is necessary to take into account the stubs and parallel lines simultaneously.

Bus lines, stub lines and connectors are expressed by three parallel distributed circuit models[2], because the crosstalk induced by adjacent parallel lines is much larger than that by the others. The propagation mode of microstrip lines is approximately quasi-TEM. Therefore, the line parameters per unit length can be calculated solving Laplace's equation by the Finite Element Method (FEM). The line parameters of connectors are measured by an impedance meter.

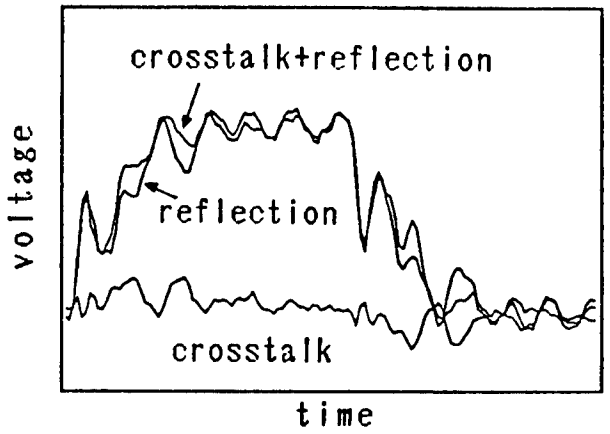


Fig.2 Crosstalk waveforms.

Transceivers are expressed by simple lumped circuit models. The equivalent circuit of an output stage transceiver is a combination of a pulse voltage source at no load V_{out}, output resistance R_{out} and capacitance C_{out}, while that of an input stage is a parallel circuit of input resistance R_{in} and capacitance C_{in}. These equivalent circuit parameters are obtained as follows[3]. The output resistance R_{out} is directly calculated using the following relationship between load capacitance C_{LOAD} and propagation delay time at the 50 percent level of an output waveform $V_{OUT}(t)$:

$$V_{OUT}(t)=Vo[1-\exp\{(t-t_{pd})/(C_{LOAD}R_{OUT})\}] \quad (1)$$

$$R_{OUT}=(t-tpd)/(0.693C_{LOAD}) \quad (2)$$

where Vo and tpd are the maximum output voltage and propagation delay time, respectively. In the following analysis, we used an average value of low to high and high to low output resistances. The other parameters were measured by an impedance meter.

Table 1 lists the line and device parameters used in the following analysis.

EVALUATION METHOD

Transmitted waveforms at the receiving end are evaluated. Figure 3 defines stable times to be evaluated. We also define three waveform conditions at the receiving end by introducing a factor α.

$$\alpha = \mathrm{Min}(T_H, T_L)/(0.5T_C) \quad (3)$$

$$\left.\begin{array}{ll} \text{Stable} & : 0.70 \leqq \alpha \\ \text{Quasi-stable} & : 0.50 \leqq \alpha < 0.70 \\ \text{Unstable} & : \alpha < 0.50 \end{array}\right\} \quad (4)$$

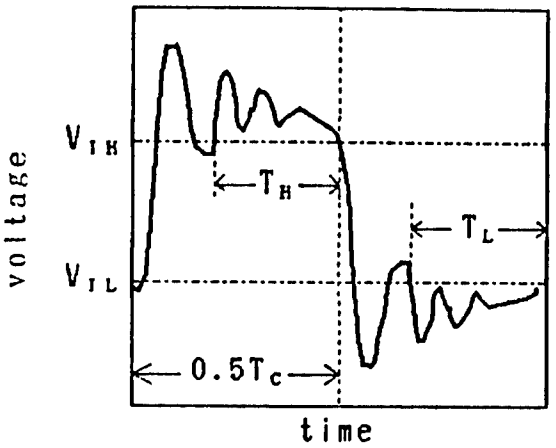


Fig.3 Stable time definition.

NUMERICAL ANALYSIS

Figure 4 shows the relationship between the number of packages and the operating frequency. Here, we can see a trade-off between them, as well as three regions corresponding to the three waveform conditions above. As the number of packages increase, the reflection, attenuation and crosstalk become large.

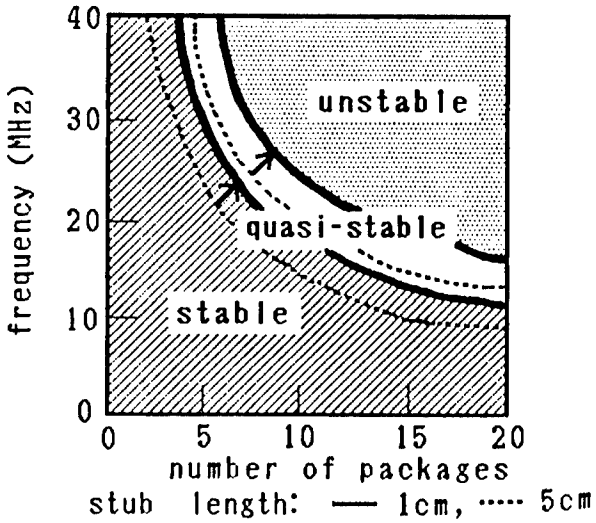


Fig.4 Relationship between the number of packages and frequency.

These noises can be reduced by lowering the operating frequencies. It should be noted that the reduction of stub length is very effective in improving of trade-off. The reason for this is that the noises decrease with a reduction in stub length. In other words, stable time increases with a decrease in stub capacitance as shown in Fig.5.

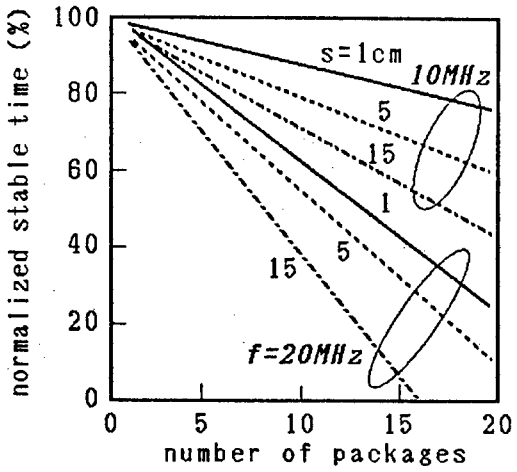
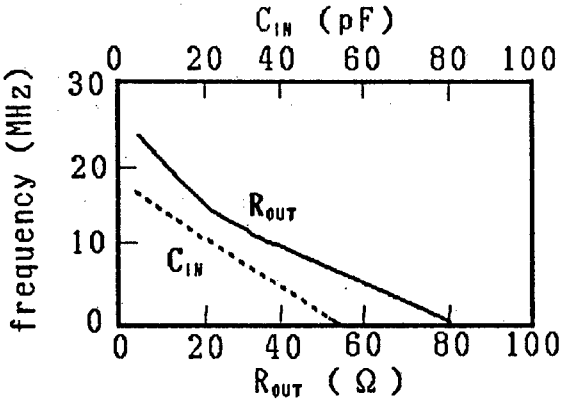


Fig.5 Relationship between the number of packages and normalized stable time.

Figure 6 shows the relationship between the output resistances of drivers, the input capacitances of receivers and



Rout variable :Cin =15pF
Cin variable :Rout=31Ω

Fig.6 Relationship between R_{OUT}, C_{IN} and frequency.

the upper stable frequencies. The reduction of output resistance and input capacitances can increase the operating frequencies and the number of packages. This increase is due to the reduction in the impedance mismatch of stub lines and the enhancement of drivabilities. In addition, Fig.7 suggests that the reduction of crosstalk at the connector pins will improve the trade-off.

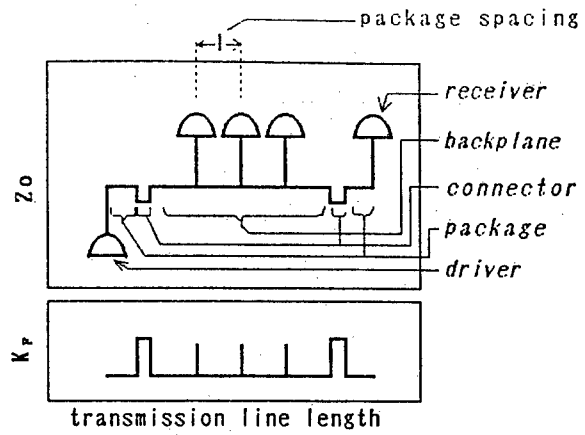


Fig.7 A profile of characteristic impedance (Zo) and forward coupling coefficient (K_F).

Figure 8 shows a comparison of the drivability between TTL and ECL-driven bus lines. The ECL drivers have a potential to improve the operating frequency more than three times since the output resistance and input capacitance of ECLs are typically six and three times lower than that of TTLs, respectively.

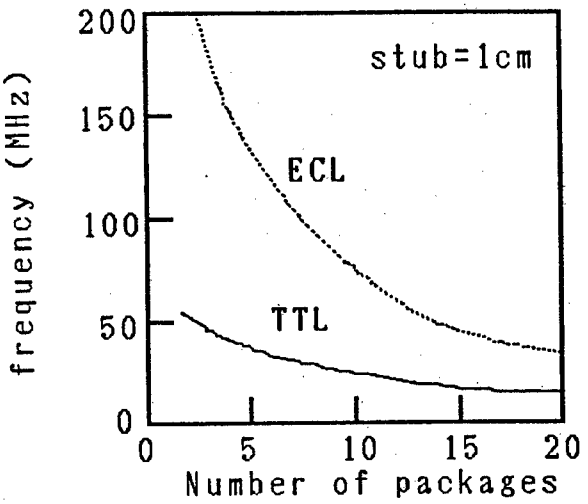
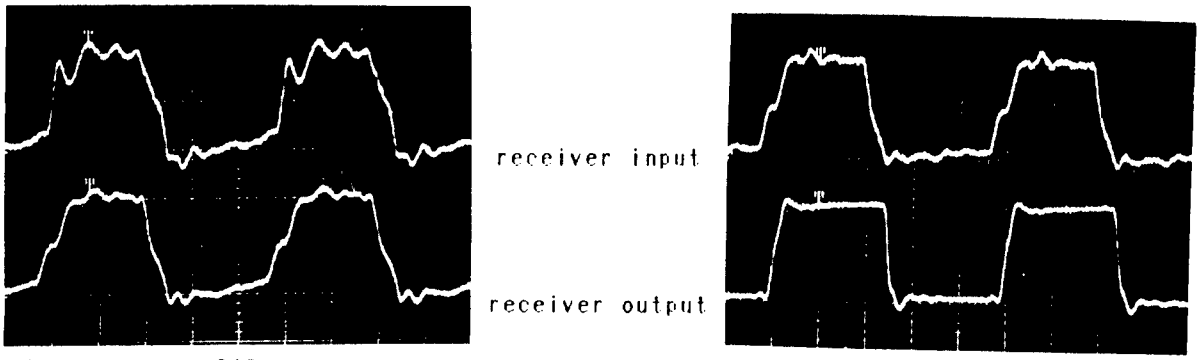


Fig.8 A comparison between TTL and ECL drivabilities.

APPLICATIONS

Numerical analysis indicates that the reduction of stub length is effective for the improvement of operating frequencies and the number of packages. Accordingly, we fabricated two types of packages to compare transmission properties. Dual-in-line (DIP) and surface mount device (SMD) transceivers are mounted on packages con-

(a) Fabricated bus line package.



(b) Transmission waveforms with 10 packages, at 20MHz.

Fig.9 A comparison of fabricated bus line packages and transmission waveforms between SMD and DIP.

nected to a backplane with high density connectors[4]. The types of both transceivers are quite the same. The dimensions and line parameters are the same as shown in Table 1.

Figure 9 shows a comparison between DIP and SMD packaging. The receiver input waveform of SMD is much better than that of DIP, and the duty of the DIP receiver output waveform is greatly changed. This is due to the difference in stub length. Since the SMD drivers mounted on both surfaces of the packages can be located in a smaller area adjacent to connectors, the stub length becomes shorter and the reflection and crosstalk noise become very small. Consequently, SMD improves the operating frequency or the number of packages by 30 percent.

CONCLUSIONS

This paper has described techniques for improving the operating speed and driving capabilities of bus lines in a bookshelf-type packaging system. We have introduced a new multi-parallel distributed circuit model with many stubs for analyzing the reflection and crosstalk noise simultaneously. Numerical analysis shows that a trade-off exists between the upper limit of speed and the number of packages. The reduction of stub length, output resistance and input capacitance will improve the trade-off. In addition, experiments indicated that reduction of stub length by surface mount bus drivers on both surfaces of a package is highly effective for achieving high operating speeds.

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ANALYSIS OF THE DYNAMIC PHENOMENA DURING LAMINATION OF MULTILAYER PRINTED CIRCUIT BOARD BY THE MEASUREMENT OF PRESSURE DISTRIBUTION

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ABSTRACT

In order to develop improved methods for manufacturing multilayer printed circuit boards (MLPCB) in the future, it is necessary to understand the dynamic phenomena which occur during the lamination process. Consequently, the authors have attempted the first study of the lamination process by the direct measurement of the pressure distribution. A pressure distribution sensor with 81 pressure detectors arrayed in a 9x9 array was developed specifically for this study. The basic structure of the pressure detector is that of a parallel plate structure instrumented with strain gauges. The array of such detectors enables the exact multipoint measurement of the dynamic pressure behavior under conditions of high pressure and high temperature. From the results of our experiments, the following conclusions can be drawn:

(1)The pressure is distributed such that the maximum pressure is located at the center of the mold. As curing progresses, the pressure gradient from the edges to the center increases, with a commensurate increase in the pressure level at the center of the mold.

(2)The final thickness of the cured MLPCB correlates well with the pressure distribution during the initial stage of curing.

(3)Theoretical models which explain the behavior noted in (1) and (2), above, have been developed. The behavior of the laminate during the initial stage of curing can be represented by the viscous fluid flow, while the cured laminate can be treated as a solid mass. The thickness variation in the cured MLPCB expresses the magnitude of the springback of the laminate, which is approximately proportional to the pressure distribution during the initial stage of curing.

INTRODUCTION

Today, with the increasing component density in electronic devices, multilayer printed circuit boards (MLPCB) with higher density and more layers are demanded. Since current lamination technology is primarily based on empirical rules, the manufacturing of MLPCB for the next generation supercomputers is becoming increasingly difficult.

The lack of a firm scientific basis for the description of the lamination process is due, in large part, to our poor understanding of the dynamic behavior during curing. Various defects that occur during lamination, for example, prepreg voids and interlayer shifting, are considered to be related to the stresses which act on the MLPCB during lamination. Because of our lack of detailed knowledge of the actual stress fields, the causes of the defects are not well understood.

We have used our special instrumentation to provide the first detailed measurement of the pressure distribution during curing and have used the resulting data to analyze the mechanism of lamination.

METHOD OF PRESSURE DISTRIBUTION MEASUREMENT

The local pressure, as defined in this paper, has the following meaning. As shown in fig.1, the total pressing force is considered to be divided between the prepreg resin (through the hydraulic pressure which develops in the liquefied resin) and the direct contact which occurs between the prepreg glass cloth and the copper foil of the circuit board. Consequently, the integrated value of the force on the detecting surface divided by its associated area is regarded as the local pressure.

For the accurate measurement of pressure distribution, the following characteristics are demanded for the sensor. First, the detecting block itself must have high rigidity. If not , the deflection of the detector will affect the measurement and the actual contact force can never be measured. Second, the detector must detect only the vertical force, with little interference from the frictional stress. Last, the sensor must be able to perform continuous multipoint measurement under conditions of high pressure and high temperature.

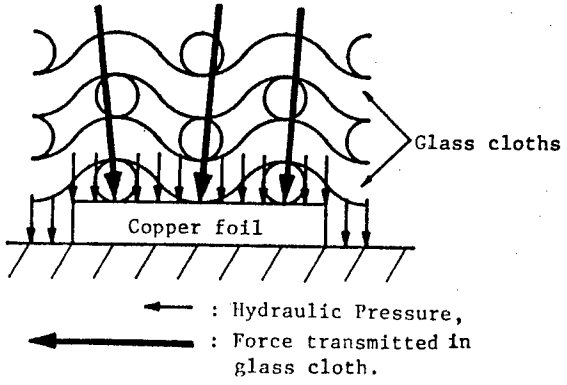

Fig.1 Composition of the total pressing force.

The basic structure for such a sensor can be a parallel plate structure as shown in fig.2. When a force is applied to the detecting block, surface tensile and compressive strains are caused by the deformation of the parallel plate structure. By converting these strains into voltage, using a strain gauge bridge circuit, the force is accurately detected. On the basis of this structure, we have developed the pressure distribution sensor shown in fig.3. The diameter of each detecting point is 8mm, and a 9x9 array of detectors has been produced on a 20mm pitch.

Fig.4 shows a typical result of the calibration of a pressure detector. Each detector shows good linearity, low hysteresis and a low level of crosstalk. In addition, the detectors perform well under conditions of up to 200℃ temperature and 10MPa pressure.

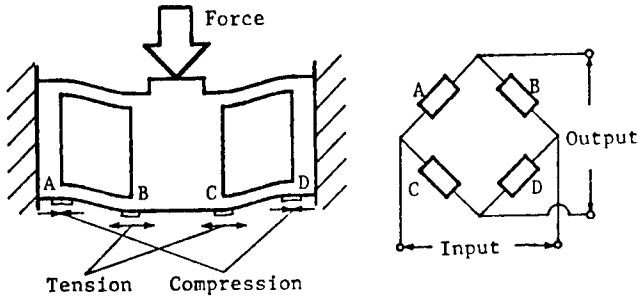

Fig.2 Parallel plate structure.

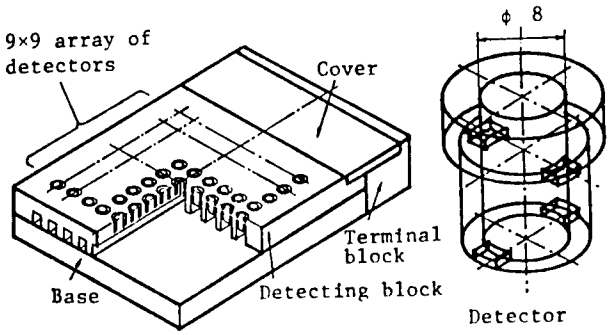

Fig.3 Pressure distribution sensor.

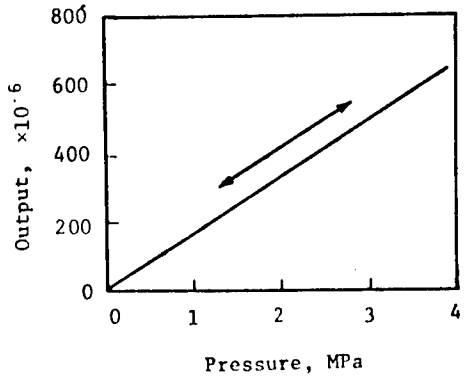

Fig.4 Example of the characteristic of the pressure detector.

EXPERIMENTAL METHOD

The experimental equipment is shown in Fig.5. The specimen is located between a jig board and the pressure distribution sensor and is heated by upper and lower heating plates. The pressure in the mold chamber can be reduced to approximately 60Torr to eliminate trapped air. A 100ton universal testing machine is used to exert lamination force on the specimen.

Fig.6 shows the constitution of the specimen used in the experiment. The 180mm square experimental specimen was cut from actual MLPCB material (polyamide prepregs and PCB substrates) and was piled up using exactly the same procedures which are employed in industrial practice: The upper and lower surfaces of the specimen were cap layers with continuous copper foils, and the inner layers were 13 etched, 2-sided PCB substrates, each separated by 2 or 3 layers of prepreg, for a total of 30 prepreg layers. Positioning pins were not used.

Fig.7 shows the temperature and load schedule of the experiment. The experiments were performed in accordance with following procedure. After aligning the specimen at room temperatue, the temperature was raised to 130℃ to melt the prepreg. At this temperature the load was applied (mean pressure of 2.5MPa and net load of 80kN). After 60 minutes, the temperature was increased to 170℃. After holding this temperature for 90 minutes to allow for complete curing, the specimen was cooled. At 50℃, the load was removed.

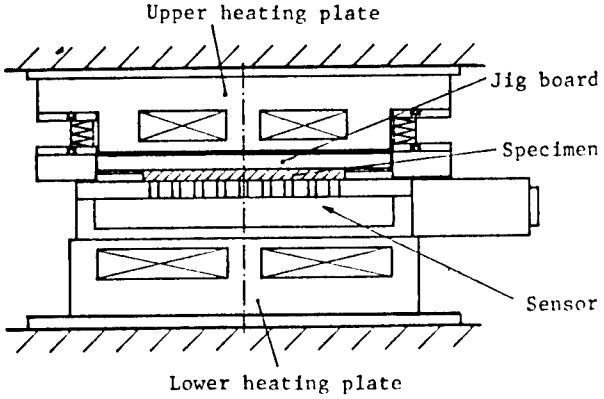

Fig.5 Experimental equipment.

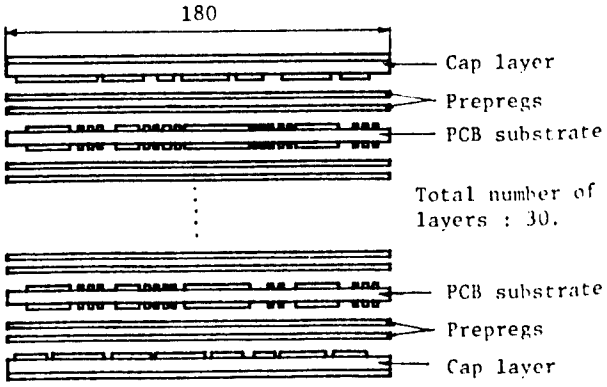

Fig.6 Constitution of the specimen.

RESULTS

An example of the typical experimental results, which were obtained, is discussed below.

Fig.8 shows the behavior of the pressure as a function of time at two representative points: the center point and the middle of the outermost edge of the specimen. As may be seen in the figure, the pressure at the center rises to a peak of 7MPa, which is about 3 times higher than the mean pressure. In contrast ,the pressure at the edge of the specimen is lower than the mean pressure throughout the lamination process.

Fig.9 shows a 3-dimensional plot of the pressure distribution at the stage just after load application (corresponding to time ① in fig.6). The appearance of the pressure distribution is like that of a hill. A few minutes later, the slope of the pressure distribution begins to become steeper, producing a more sharpened shape. Fig.10 shows the pressure distribution at the stage just after the temperature was increased from 130°C to 170°C (corresponding to time ② shown in fig.6). After this point, the pressure distribution did not show a drastic change until unloading. Finally, at the start of unloading, the pressure was first released around the edge of the specimen. The pressure remained high at the center of the specimen until the very end of unloading. Fig.11 shows the pressure distribution during the unloading process when the total load had been reduced to 10kN (corresponding to time ③ in fig.6).

Fig.12 shows the thickness variation in the cured specimen of this experiment, expressed as the deviation from the thickness of its thinnest part (4.03mm). The specimen is thick at the center and thin around the edge.

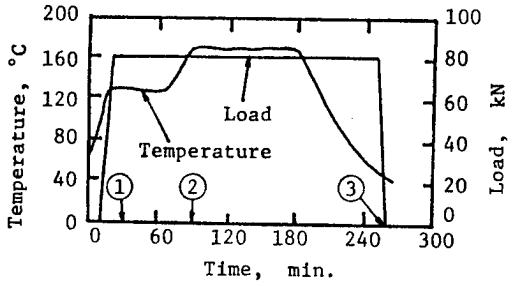

Fig.7 Temperature and load schedule.

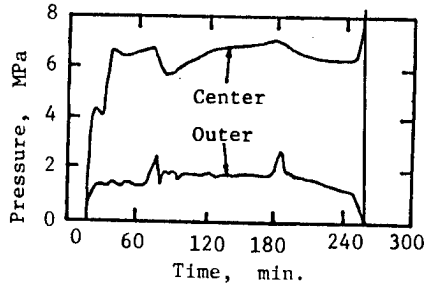

Fig.8 Pressures at representative points.

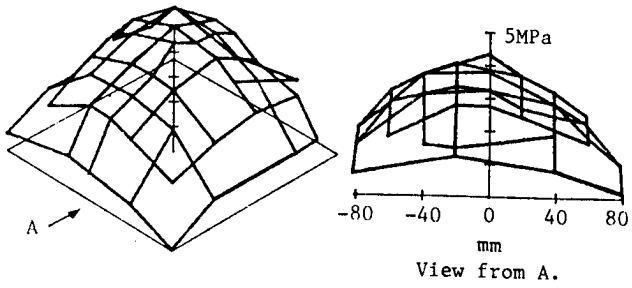

Fig.9 Pressure distribution at time ①.

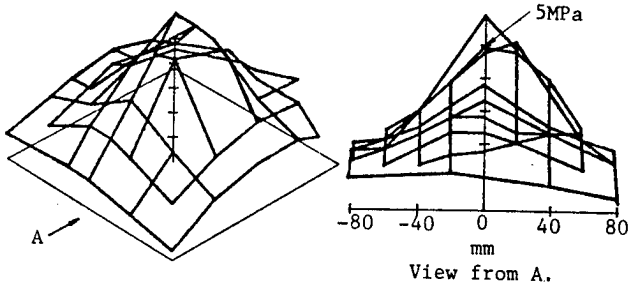

Fig.10 Pressure distribution at time ②.

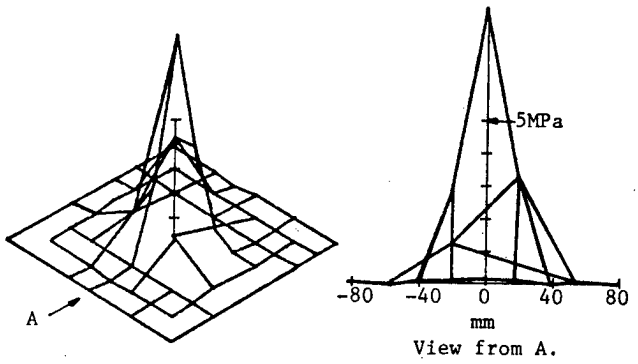

Fig.11 Pressure distribution at time ③.

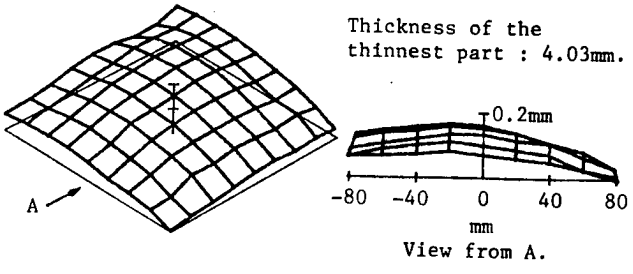

Fig.12 Thickness variation in the cured specimen.

DISCUSSION

The dynamic change of the pressure distribution in the laminate during curing is considered to be due to the phase transition of the prepreg resin.

It is suggested that the initial hill-shaped pressure distribution is produced by the pressure in the liquefied prepreg resin itself, or is closely related to it. When the load is applied, the prepreg resin flows out through the extremely narrow gaps between layers. At this time, due to the viscosity of the resin, the hydraulic pressure of the prepreg resin will become high at the center and lower around the edge. This suggested mechanism is supported by the results of a recent study of the causes of void generation in the curing of prepreg [1]. One important cause of void generation is the vaporization of solvent from the resin, which is caused by low pressure in the liquefied prepreg resin. Corresponding to our finding of low pressure around the edge of the specimen, most voids are observed, in practice, around the edge of MLPCB. In addition, change in the pressure implies the presence of viscous shear stress, which will deform the PCB substrates and cause interlayer shifts. This shifting is a major obstacle in the manufacturing of high density MLPCB. Consequently, for the prevention of void and interlayer shift generation , it is suggested that mold cavities should be designed to produce a more uniform pressure distribution in the initial stage of pressing.

The sharp gradient pressure distribution, which results after curing has progressed, looks like the so-called friction hill in the case of plastic forming. In this case, the pressure is considered to be transmitted by both the cured prepreg resin and the glass cloth, and the frictional forces between the laminate and the jig board begin to dominate. The frictional forces generate shear stresses in the cured MLPCB, which also tend to cause interlayer shifting. Consequently, it is desirable to develop a method of reducing the frictional forces between the jig board and the laminate.

The concentration of the pressure at the center of the specimen during the unloading process is considered to be due to the elastic springback of the specimen. As shown in fig.13, during the unloading process, the specimen expands in the vertical direction and contracts in the horizontal direction. In this way, the specimen follows the elevation of the jig board and maintains pressure between the jig board and the laminate. The magnitude of the springback will appear as the actual variation in the final thickness of the cured specimen, which correlates well with the pressure distribution during the initial stage of curing.

The basic phenomena observed in these model experiments are considered to be affected most significantly by the following factors:

(a)The mechanical deformation characteristics of the specimen. For example, the coefficient of viscosity of the resin.

(b)The frictional coefficient between the specimen and the jig board.

(c)The geometory and constitution of the specimen. For example, the dimensions , the number of layers and materials which are used in the specimen.

(d)Mechanical restrictions on the motion of the specimen. For example, the presence and location of positioning pins.

In the application of the results of the experiments which are reported herein, we should pay attention to the abovementioned factors.

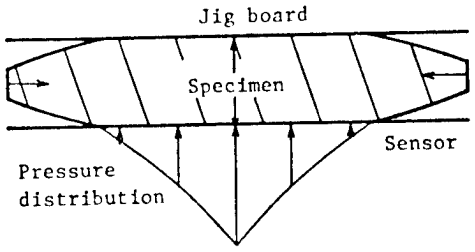

Fig.13 Behavior of the specimen during unloading process.

ANALYSIS

The two characteristic aspects of the pressure distribution, the hill-shaped aspect and the sharpened one, may be explained by models as follows.

The radial flow of resin between the layers during the loading process can be approximated by the Newtonian fluid flow between parallel plates as shown in fig.14. Considering the forces acting on an infinitesmal, fan-shaped element in the flow, which are due to viscous shear stress and pressure, the equation shown below can be obtained.

$$P = 2\,Pm\,\frac{R' - r'}{R'}$$

where, Pm : Mean pressure,
R : Total radius of the flow field,
r : Distance from the center.

This equation describes a parabolic pressure distribution. According to this equation, the ratio of the pressure at the center point to the mean pressure becomes 2:1 regardless of the total radius of the flow. This suggestion, which results from the theoretical model, agrees with the experimental result.

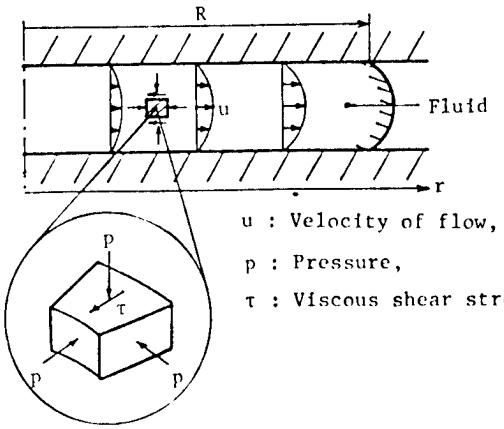

Fig.14 Newtonian model of resin flow.

On the other hand, when the resin is cured, the specimen can be approximated as a solid mass as shown in fig.15. Once again considering the forces acting on a fan shaped element, which are frictional stress and normal stress, the equation shown below can be obtained.

$$P = Pc \exp\left(-\frac{2\mu}{k\,h} r\right)$$

where, Pc : Pressure at the center point,
μ : Frictional coefficient,
k : Lateral pressure coefficient,
h : Height of mass,
r : Distance from the center.

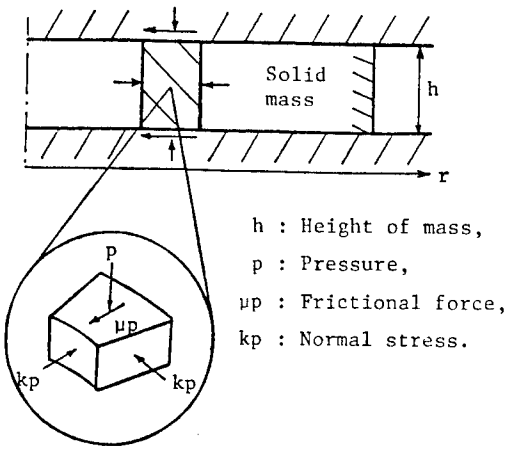

Fig.15 Solid mass model of the cured laminate.

This equation expresses an exponential pressure distribution. According to this equation, the pressure gradient becomes steeper, as the frictional coefficient increases. The pressure gradient is determined by the magnitude of the coefficients μ and k, which are characteristics of the materials of the MLPCB and the jig board. Consequently, it is concluded that the ratio of the pressure at the center point to the mean pressure will increase, as the size of the laminate increases. This ratio was about 3:1 in the experimental case, but it may become much larger in the industrial practice, because the size of the actual MLPCB material is about three times as large as that of the experimental specimen.

The dependence of the final thickness of the cured laminate on the pressure distribution during the initial stage of curing may be explained by the following model. Fig.16 shows the mechanism of the elastic springback of the laminate.The forces acting on the element ① and ② just before unloading can be considered as follows. The element ① is restricted by the compressive stresses in both the vertical and the horizontal direction. On the other hand, the element ② is restricted also by the compressive stress in the vertical direction, but by the tensile stress in the horizontal direction, which is due to the contraction of the laminate by cooling. Consequently, the apparent coefficient of elasticity in the vertical direction becomes larger in the case of the element ① and smaller in the case of the element ②. In this way, the actual magnitude of the elastic springback will become not the solid but the broken curve. Because the approximate appearance of the pressure distribution during curing is determined by that just after load application, the thickness variation in the cured MLPCB, which results from the elastic springback, will correlate well with the pressure distribution during the initial stage of curing.

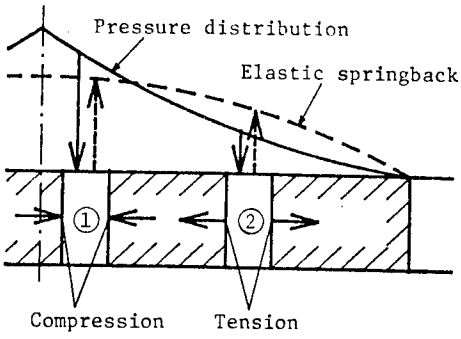

Fig.16 Elastic springback mechanism of the cured laminate.

CONCLUSIONS

A pressure distribution sensor using a parallel plate structure has been developed, which has good performance under conditions of high temperature and high pressure. The following conclusions were derived from the results of our experiments:

(1)The pressure is distributed such that the maximum pressure is located at the center of the laminate. As curing progresses, the pressure gradient from the edges to the center increases, with a commensurate increase in the pressure level at the center.

(2)The final thickness of the cured MLPCB correlates well with the pressure distribution during the initial stage of curing.

(3)Theoretical models which explain the behavior noted in (1) and (2), above, have been developed. The behavior of the laminate can be represented by the viscous fluid flow during the initial stage of curing, while the cured laminate can be treated as a solid mass. The thickness variation in the cured MLPCB expresses the magnitude of the elastic springback of the laminate, which is approximately proportional to the pressure distribution during the initial stage of curing.

ACKNOWLEDGEMENTS

The authors would like to thank Prof.Dr. T.Nagao of Tokyo Univ. for useful discussion, Toko Co. Ltd. for manufacturing of pressure distribution sensor.

REFERENCE

[1]H.Murooka, M.Kyooi and H.Murakami, "Voids in Multilayer Printed Circuit Boards by Thermal Pressing Adhesion: A Study of Causes", Preprint of Spring Conf. of Jpn.Soc.Pla.Eng., 1988.

MOISTURE RESISTANCE OF EPOXY RESIN USED FOR EXTREMELY LOW PROFILE IC MODULES

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1. Abstract

Since IC CARDS and TAB represent extremely low profile IC MODULES, it is difficult to realize such package forms at high moisture resistance. In this report, we have evaluated three different types of epoxy resins (pellet, liquid, and solvent type) which suit automated and IN-LINE processes. We have also considered problems regarding reliability and process control, and have obtained the following result.

Moisture resistance is good in the epoxy resins of the pellet, solvent and liquid types, in that order, because the liquid epoxy resin liberates a lot of CI ions due to the production process of the main epoxy resin and the design of composites. The pellet type resin contains many fillers, and as a result moisture diffusion into the bulk resin is low., in the case of the liquid type resin using acid anhydride hardeners epoxy resin it is important to minimize the moisture absorption during idling time between coating and curing.

2. Introduction

Miniaturized IC packages have been strongly requested, and extremely low profile IC modules such as less than 0.5 mm in total thickness have been developed. Fig. 1 shows a TAB (tape automated bonding) package (an extremely low profile IC module is typical). Each TAB package consists of chip, tape (polyimide) and sealing resin less than 0.1 mm in thickness. Table 1 shows comparison of extremely low profile IC module sealing resins currently used. The pellet type resin is solid, and its moisture resistance can be improved by amine type hardener. However, there are some disadvantages, such that the workability is not good and the curing time is rather long. The liquid epoxy type resin is liquid to answer requirements of improving sealability and workability, and liquid acid anhydride is often used as a hardener. The solvent type resin is solid resin to be dissolved by a solvent, and the sealability and workability can be improved by

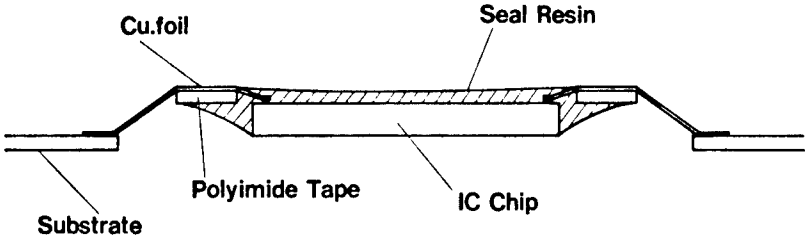

Fig. 1 Extremely Low Profile IC Module(TAB)

Table. 1 Characteristics of The Evaluated Resins

		Pellet type	Liquid eoxy type	Solvent type
Composition	Epoxy resin	Bisphenol type	Bisphenol type	Bisphenol type
	Hardener	Amine type	Acid anhydride	Phenol novolak
	Cure accelerator	Amine type	Amine type	Amine type
	Colorant	Carbon black	Cardon black	Carbon black, dye
	Filler	SiO2(≒70%wt)	SiO2(≒10%wt down)	SiO2(≒10%wt)
	Solvent, Dilvent	———	Epoxy monomer	Organic solvent
Workability	Property	Solid	Liquid	Liquid
	Low profile	△	○	◎
	Flowability	△	○	○
	Cure condition	150°C*15hr	100°C*1hr+150°C*3hr	Final 150°C*1hr
Application		Standard COB	Thin type COB, TAB	Thin type COB, TAB

adjusting the solvent in volume. Few comparison data on moisture resistance of these sealing resins is available. We have compared the moisture resistance of extremely low profile sealing resins and examined factors affecting the moisture resistance. An in-line operation in the sealing process or an idling time from the potting operation to the curing operation is a very important factor for the moisture resistance. We have examined effects of the idling time.

3. Experiment and results

3.1 Comparison of moisture resistance of sealing resins

Experimental method

A comparison of moisture resistance of the sealing resins in Table 1 has been done under the HAST conditions (at 120°C, 85% RH, and bias voltage of 10 V) using the TEG patterns (Al-Si parallel patterns, 7μm in width, 2μm in gap, no passivation). To examine causes of the effects, we analyzed extracted ions and made various experiments by setting a level for the filler amount.

Results

Fig. 2 shows the Weibull distribution diagram of comparison of the sealing resins. The order of higher moisture resistance is pellet type resin, solvent type resin, and liquid epoxy resin. In the case of pellet type resin and solvent type resin, the cathode is degraded, and grain boundary type aluminum corrosion can be seen on its surface. In the case of liquid epoxy resin, the anode is degraded, and aluminum pitting corrosion can be seen on its surface.

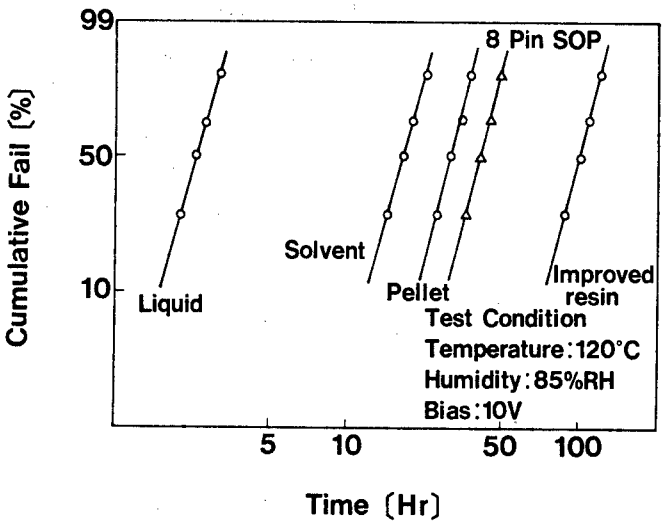

Fig. 2 Weibull Plot Result at HAST Condition

Results

Fig. 3 shows the HAST evaluation results. The moisture resistance decreases as the idling time increases, and the anode is degraded and aluminum corrosion can be seen on its surface. Fig. 4 shows the PCT evaluation results. Cracks on the resin surface increase in number as the idling time increases.

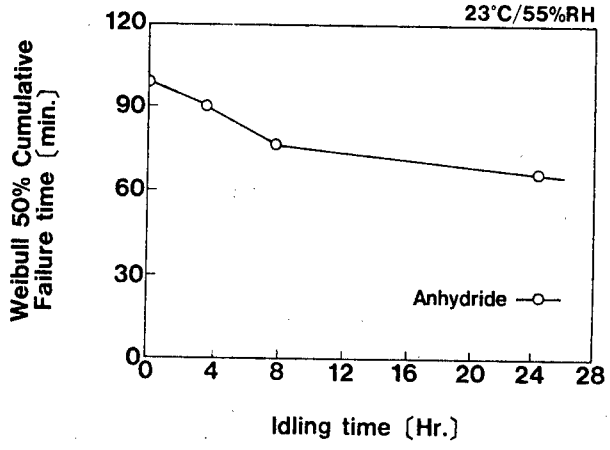

Fig. 3 HAST Results vs. Idling time

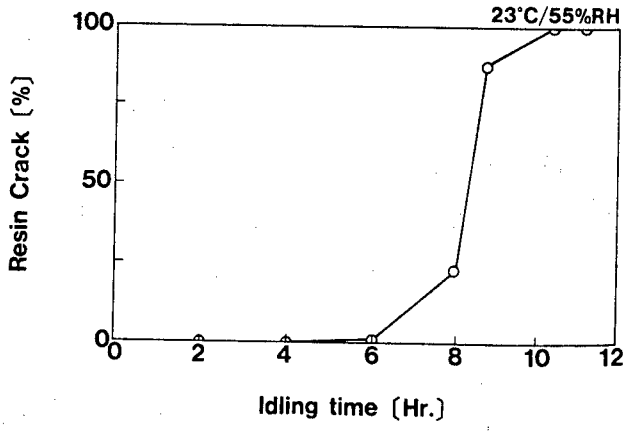

Fig. 4 Resin Cracking at Pressure Cooker Test (121°C/100%RH) vs. Idling time

Fig. 5 shows the extracted ion analysis (condition: Boiling wafer for 20 Hr.) that Cl ions increase as the idling time increases. The thermal analysis shows that, as shown in Table 3, the reactivity during gelation decreases and the glass transition temperature of the cured resin lowers as the idling time increases. To examine the effect of the idling time on the molecular level, the FT-IR analysis has been made. The result shows that the acid anhydride, which is one of the composition, is hydrolyzed.

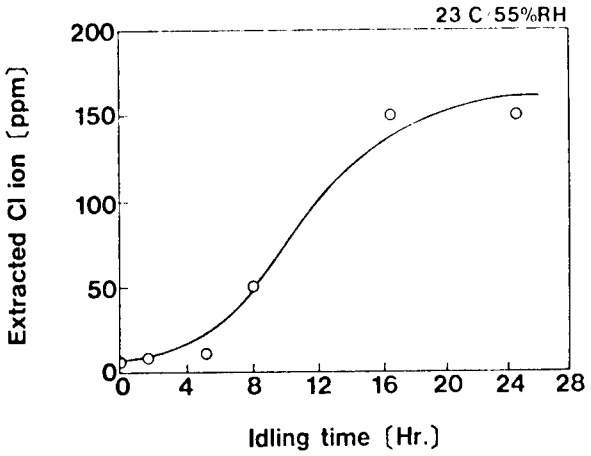

Fig. 5 Extraction Characteristics of the Evaluated Resins. vs. Idling time

Table. 3 Results of thermal analysis

		Idling time (Hr.)		
		0	4	8
Acid anhydride type	ΔQ (mj/mg)	44	37	25
	Tg (°C)	138	127	121

Table 2 gives the extraction characteristics of each sealing resin. The measurement conditions are as follows: Each sealing resin is cured under the specified conditions, and the cured resin is crushed, then extracted at 121°C and 2 atmospheres for 20 hours. The amount of ion impurities is measured with an atomic absorption spectro photometer and an ion chromatographic apparatus. The PH value and electric conductivity (EC) of extracted water are measured with a PH meter and a conductivity meter. In the case of liquid epoxy resin, a very large amount of Cl^- ions is detected. The electric conductivity (EC) of extracted water is highest.

Table. 2 Extraction Characteristics of The Evaluated Resins

		Pellet Type	Liquid Type	Solvent Type
E.C(μs/cm)		44	79	11
PH		4.7	4.2	5.0
Extraction IONS(ppm)	Na	3.4	2.0	6.9
	K	1.1	0.4	2.6
	Cl	34	193	12
	F	7.5	2.0	13

3.2 Effects of the idling time on the moisture resistance of liquid epoxy resin.

Experimental method

Samples have been prepared by potting the liquid epoxy resin type (acid anhydride hardener) and setting idling times under the specified conditions (at 23°C and 55% RH). The test has been conducted under the HAST conditions (at 120°C, 85% RH, and bias voltage of 3 V) using the previous mentioned TEG and under the PCT conditions (at 121°C and 100% RH) using actual devices. To try to find the cause, an extracted ion analysis, thermal analysis, and FT-IR analysis have been made.

4. Discussions

Low moisture resistance of the liquid epoxy resin is considered to be caused by a lot of Cl^- ions contained in the resin because the aluminum used this resin is the anode degradation type in the corrosion mode. An increase in Cl^- ions may be caused by excessive amount of epichlorohydrin used for liquid epoxy resin manufacture or by the curing condition and accelerator. For example, bisphenol epoxy resin can be produced by reacting bisphenol and epichlorohydrin under the alkaline condition (Fig. 6). To produce low-molecular epoxy resin to be used for liquid epoxy resin, an excessive amount of epichlorohydrin is required. During reaction, chlorhydrin ether is formed as a subproduct. Cl^- ions are liberated from unreacted epichlorohydrins or subproducts of chlorhydrin ether, by the hydrolysis or accelerator during heating.

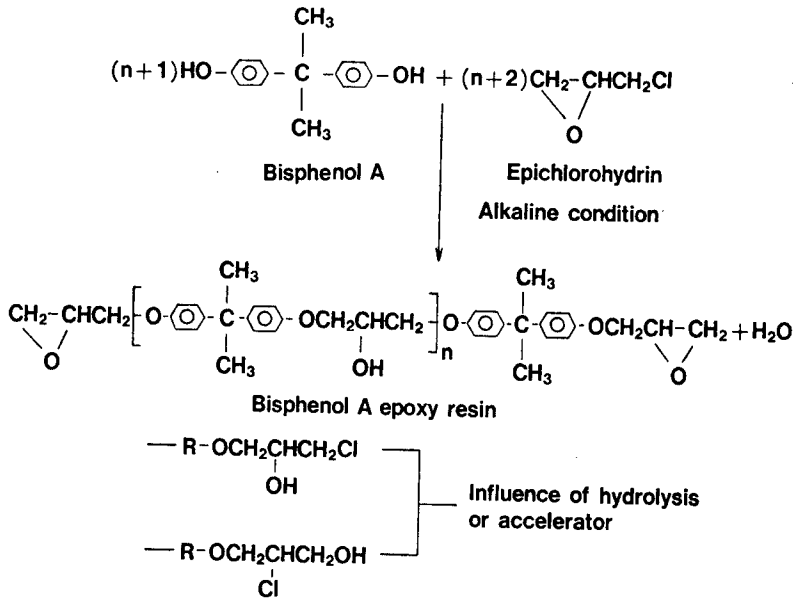

Fig. 6 Method to manufacture of bisphenol A epoxy resin

The fact that the moisture resistance of the pellet type resin is higher than that of the solvent type resin is considered to be caused by a difference in the filler amount. The improved resin in Fig. 2 is the filler rich solvent type resin (70wt%). As seen in Fig. 2, the improved resin shows that as the filler amount increases, the moisture resistance becomes longer and also higher than that of the transfer sealing resin (8p SOP). This degradation mode is also the same cathode as the solvent type resin. A difference in the filler amount influences the moisture diffusion phenomenon, the main factors of the corrosion, because the corrosion mode is the cathode degradation type.

The main cause of degradation of the moisture resistance of the liquid type resin by the idling time in the sealing process is considered to be hydrolysis of the anhydride caused by moisture absorption of the hardener. Carboxylic acid formed by hydrolysis may decrease the reactivity under the same curing condition.

(① An increase in activation energy during reaction, ② a decrease in activation of the accelerator, ③ acceleration of secondary reaction). As a result, the dedicated curing material characteristics cannot be obtained, and free ions increase in quantity due to a decrease in resin hardness and a reduction in bulk moisture resistance. These phenomena may cause cracks on the resin surface and accelerate aluminum corrosion during the moisture resistance test.

5. Conclusion

We have examined, in this experiment, the basic moisture resistance level of extremely low profile IC sealing resins, factors affecting the moisture resistance, and effects of the idling time (effects of absorbed moisture) in the sealing process. The moisture resistance greatly depends on the resin type, and the idling time greatly affects the moisture resistance depending on the resin type. The resin to be used should be carefully selected, and the process should be deliberately set.

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ADHESIVELESS POLYIMIDE LAMINATE AS A CIRCUITRY MATERIAL

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ABSTRACT

Many developments have been required in silicone wafer, IC packaging, PCB substrate and whole system for hi-speed computer. In substrate, shorter wiring path of PCB and lower dielectric constant of substrate will bring higher processing speed of computer. Wiring path of PCB has been rapidly minimized by multi-layer wiring technology.

However, few low dielectric constant materials go into commercial use for multi-layer PCB in computer applications. The major reason of their inavailability is due to the trade-off between dimensional stability and low dielectric constant. For example, PTFE-glass material with its very low dielectric constant (ε-2.8) cannot satisfy the dimensional stablilty requirement of high aspect ratio through-hole after multi-lamination.

Recently we have developed brand-new materials for multi-lamination with both of low dielectric constant and excellent dimensional stability. These materials can realize higher processing speed and higher wiring density by applying a conventional multi-lamination process.

INTRODUCTION

Multi-layer PCB is widely applied as a substrate for large scale computers. As the demand for higher processing speed grows, higher propagation speed of the substrate is strongly requested. Generally speaking high propagation speed in multi-layer PCB can be attained by its lower dielectric constant property.
Almost conventional FPC materials are three layers construction: copper/adhesive/polyimide. Having the adhesive layer, these laminates cannot give full play to the excellent character of polyimide layer.

Many investigations have been made of adhesiveless two layer materials. The leading approaches are direct casting of polyimide varnish on metal foil, metal vapor-deposit over polyimide film and plating. We adopted the casting method and succeeded in the considerable testing of quantity production.

In this paper we intend to report mechanical and electrical characteristics of the adhesiveless FPC (A-1 FPC). And some interesting applications are also reported.

THEORETICAL

The main problem encountered in casting method is the residual stress which is induced by the shrinkage of polyimide layer. The residual stress gives rise to curing, wrinkle and unsufficient dimensional stability after etching process.

The shrinkage occurs at two steps. The first step is solvent vaporization and imidization of casted polyamic acid varnish on copper foil The second step is cooling after high-temperature imidization. Sufficient rearrangement of polymer chain is required to reduce stress at the first vaporization imidization step. A principal solution for the problem of polymer rearrangement is fine control of drying and heating process.

Complete imidized layer is needed to C.T.E. matching with copper foil for the second cooling step. Molecular design of polyimide is an appropriate answer to the problem.

RESULT AND DISCUSSIONS

General characteristics of the A-1 and conventional FPCs are shown in Table 1. New product is superior to the conventional product in wetar absorption and ionic impurities. Therefore, copper migration can hardly occur. Dimensional stability of the new product is also superior to the conventional one. New product can be used in fine pattern processing.

Having the adhesiveless construction, new product showed the excellent heat resistance in the 200°C, 100hrs treatment, while conventional product blancked by the carbonization of the adhesive layer. Thermal decomposition behavior of the materials are observed by thermogravimetric analysis. A-1 FPC is superior to conventional one.

THEORETICAL

Propagation speed is determined by equation (A).

$$v = c / \sqrt{\varepsilon_r} \quad \ldots (A)$$

v : Propagation speed
c : Light velocity
ε_r: Dielectric constant of material

In Table 1 you can see typical of various materials.

Table 1

Material	ε_r
E glass	6.2
Epoxy resin	3.7
Polyimide	3.4
PTFE	2.2
Epoxy/fibre glass	4.9
Polyimide/Fibre glass	4.6
PTFE/fibre glass	2.7

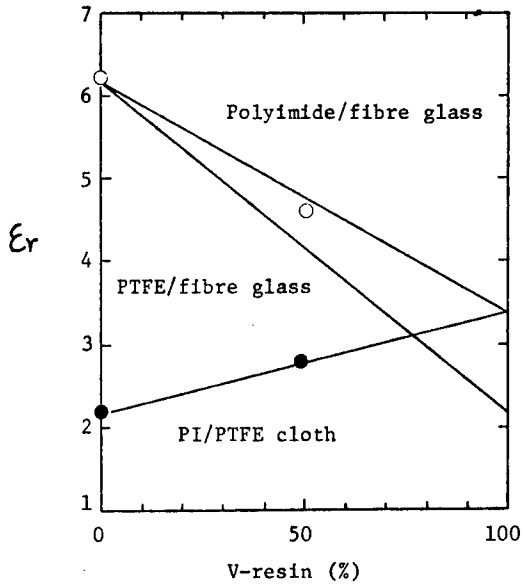
ε_r of a laminate, in other words ε_r of an insulation layer, would be roughly calculated by equation (B).

$$\varepsilon_r\text{-lami} = \varepsilon_r\text{-resin V-resin} + \varepsilon_r\text{-ref V-ref} \quad (B)$$

ε_r-lami : ε_r of laminate
ε_r-resin: ε_r of matrix resin
V-resin : Volume ratio of matrix resin
ε_r-ref. : ε_r of reinforcement material
V-ref. : Volume ratio of reinforcement material

In graph 1 some calculation results and actual data are plotted. The graph shows that a dielectric constant around 2.8 would be obtained with 50 vol% PTFE as a reinforcement material. 50 vol% of reinforcement material is the same as that of typical epoxy/fibre glass. Therefore, we concluded that 50 vol% of PTFE would not damage the prepreg's processability in multi-lamination.

Graph 1



We selected polyimide as the matrix resin in order to attain good thermal properties. The key issues in this case are affinity adn adhesion between the PTFE fibre and the matrix resin. PTFE has almost no adhesion with other materials, so some surface treatment is necessary for adhesiion improvement.

Although various chemical treatments have been used for PTFE, we adopted plasma treatment which we think is suitable for continuous treatment of fibre-cloth. In addition, multi-filament yarn is applied in order to achieve good adhesion by increasing the surface area of PTFE cloth.

EXPERIMENTAL

We have performed an experiment through prepreg to multi-PCB evaluating the following properties.

I. Prepreg

Prepregs were arranged by usual treatment. PTFE cloth was wovenfrom plasma treated multi-filament yarn to a thickness of 60-100 m and was impregnated by an originally developed polyimide varnish. In this step we observed how the polyimide reacted with the PTFE cloth. Some cloths, especially without surface treatment, could not go through to the next step because good prepregs were not available.

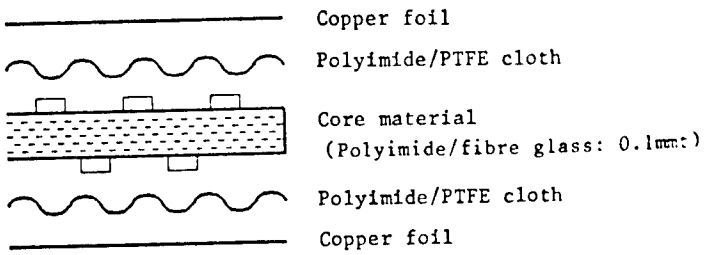
II. Laminate

Prepregs were laminated in a typical platen press process into a double-sided copper clad laminate. Here we evaluated dielectric properties, solderability and bond strength by JIS C-6481.

III.Multi-PCB

Multi-lamination behavior and processability in drilling and plating were evaluated. Dimensional stability was measured separately by fabricating a test specimen with a construction as shown in Fig. 2.

Fig. 2



Result and Discussions

I. Prepreg and Laminate

Table 2

Items	Experiment #1	Experiment #2	Experiment #3	Control(Polyimide/E glass)
*Characters of cloth				
Thickness	100	100	60	100
Type of yarn	Multi-filament	-ditto-	-ditto-	-ditto-
Surface treatment	None	Plasma	Plasma	Silane coupling agent
*Prepreg property				
Resin immersion to cloth	N.G.	Good	Good	Good
Resin amount (vol%)	-	50	50	50
*Laminate				
Dielectric constant	-	2.8	2.8	4.6
Dissipation factor	-	0.012	0.010	0.020
Solderability	-	Good	Good	Excellent
Bond strength (kg/cm)	-	1.0	1.0	1.2

(1) PTFE showed no affinity to polyimide in treatment process. Polyimide varnish could not 'wet' PTFE cloth at all and was left on the surface of the cloth in a shape of "rain-drops". (Experiment #1)

(2) Plasma treatment enhanced the affinity between PTFE and Polyimide. At the same time, we got significant data in laminate properties from plasma treated PTFE. (#2 & #3)

(3) When applied to multi-layer PCB, thin prepregs are more beneficable than thick ones. So, we evaluated Multi-PCB properties only in 60 m thickness PTFE cloth. (#3)

II. Multi-layer PCB

Table 3

Items	Polyimide/PTFE cloth	Polyimide/E glass
Behavior in laminating process	Good	Good
Dimensional change of core material(%)	X -0.020	X 0.024
	Y -0.025	Y -0.025
Processability in drilling & plating	Good	Good
Expansion in Z-axis (RT 260°C / %)	5	2 - 3

(1) #3 prepregs showed good resin filling into openings of signal and power/ground copper circuits.
(2) Dimensional change of core materials is affected by prepreg properties next to chem. PTFE prepreg showed better isotropic character than conventional glass prepreg. The result seems to be that PTFE cloth gives less stress to the core material than glass cloth does because of its low modulus.
(3) Photo 1 shows good processability of PTFE as same as common FR-4 in drilling and plating.
(4) Although PTFE cloth shows twice the expansion in Z-axis as FR.4, stress in the plated through-hole is con-sidered smaller than that of FR-4 because of its low modulus.
(5) From these results we can recommend the application of PTFE prepreg for computer substrate as shown in Fig. 3.
(6) Multi-layer construction of Fig. 3 is easily laminated and processed through conventional multi-PCB process.

Fig. 3

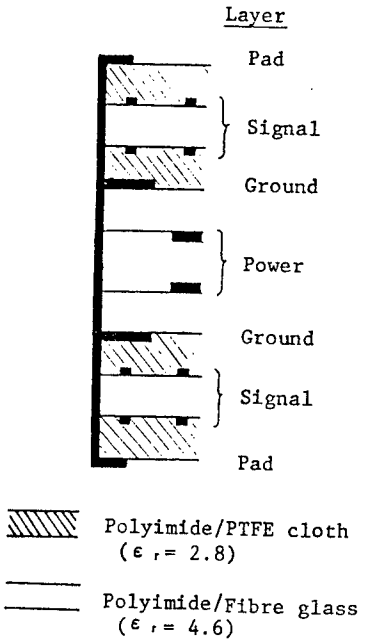
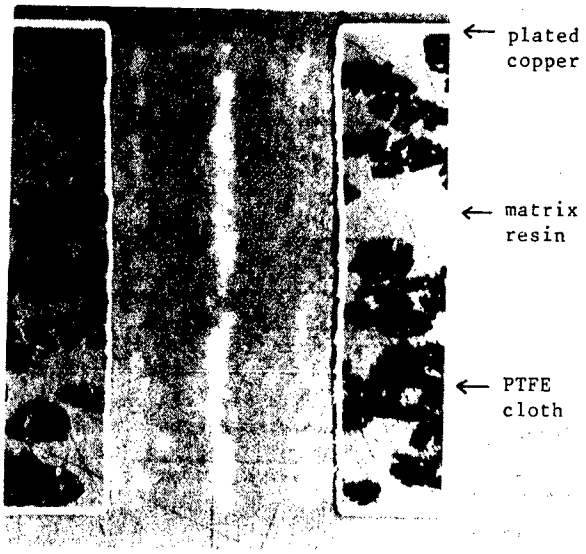


Photo 1



CONCLUSION

(1) We developed a new prepreg from polyimide resin and PTFE cloth which shows low dielectric constant ( ) of 2.8.

(2) This prepreg is easily processed into multi-PCB with conventional methods and equipments.

(3) Multi-PCB from this prepreg will bring high performance as substrates for high speed computers.

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NEWLY IMPROVED POLYMER ALLOY SYSTEMS FOR PRINTED WIRING BOARDS

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ABSTRACT

A new laminating resin system by using polymer alloy technologies was investigated to meet increasing demands on high density of the printed wiring boards.

Basic approach was carried out on thermoplastic and thermosetting polymer alloy systems. Two kinds of combinations of linear, phenoxy resin and thermosetting epoxy resins were employed and characterized to get synergetic qualities of the resin systems. By the similar structural combination, better mechanical properties were achieved when the content of phenoxy resin was not above 30%. No phase separation was observed in this region. The results of gel fraction and crosslinking density of the systems support the speculation that the linear chains of phenoxy resin are interpenetrated into the network chains of the epoxy resin. Another combination of heat resistant epoxy resin and phenoxy resin had a tendency to decrease the content of phenoxy resin for getting homogeneous structure. Adequate content of phenoxy resin in heat resistant epoxy resin was decided to get better mechanical properties.

INTRODUCTION

The blooming growth of the electronics industry has led to increasing demands for printed wiring boards with higher density, and upgraded performance. This move towards printed wiring boards has accelerated to increase the need for materials offering better dimensional stability and higher heat resistance over conventional brominated epoxy resins, which have been preferably used much higher in volume than other thermosetting resins.

We have studied the heat resistant multi-functional epoxy resins for wiring board materials in order to meet these requirements. They exhibit high glass transition temperature with low thermal expansion coefficient. It is however known that they are too brittle for wiring board materials. It is therefore important to get improved mechanical properties without sacrifice of good thermal properties. For this purpose, we have taken note of the polymer alloy combination which consists of thermosetting heat resistant epoxy resins and linear polymer.

In this paper, basic approach was carried out on two kinds of combinations by linear, phenoxy resin and thermosetting epoxy resins.

Mechanical and morphological properties were discussed in order to get synergetic qualities of the resin systems.

EXPERIMENTAL

Materials

Samples of polymer alloy systems were prepared from two kinds of epoxy resins and curing agents with phenoxy resin (PKHH from Union Carbide Corp.). The resins were obtained commercially.

We prepared the resin compositions as follows:

(1) Bisphenol-A type epoxy resin (Epikote 828) , p,p'-diamino diphenyl methane (DDM) and various contents of phenoxy resin.
(2) Multi-functional epoxy resin, phenol resin and various contents of phenoxy resin.

For the preparation of polymer alloys, methyl ethyl ketone was adopted as a solvent which adjusted the viscosity of resin formulation. These blends, known as varnishes, impregnated in woven glass cloth. The solvents in the cloth impregnated by the varnishes were completely evaporated in a treater. The prepreg obtained was vacuum-pressed at 180°C for 90min. And the resin removed from the cloth was also vacuum-pressed under the same condition as the prepreg. Thus we obtained the samples.

Characterization

The conversion of the epoxy group was determined by the method of Simazaki(1); a solution made up of 0.2N pyridine-hydrochloride, isopropyl alcohol and distilled water in the ratio of 2:2:1 were refluxed over the sample chips for 4h and then the swollen samples were titrated with 0.5N sodium hydroxide.

Gel measurement was carried out by using tetrahydrofuran as a solvent in a manner similar to Kenyon and Nielsen (2). The samples were kept in the solution for 3 weeks at room temperature,

changing the solvent every 4 days. And then the samples were dried under vacuum condition at 80°C until the weights of the samples were saturated. Gel content of the samples was estimated by comparing the initial weight with the gel weight.

Dynamic mechanical properties were measured with a torsion pendulum (RD-1100AD Rhesca Co.,Ltd.) in free vibration at less than 3.0Hz frequency at temperature ranged -130°C to 250°C.

Some initial observations on fractured surface of specimens were carried out with a scanning electron microscope (JEOL JDM-T20).

Mechanical analysis was carried out by using high impact tester (RIT-8000, Rheometrics Co,.Ltd.) and tensile shear tester (Autograph IS-5000,Shimadzu Co,.Ltd.).

RESULTS AND DISCUSSION

Bisphenol-A type epoxy resin alloy systems

Bisphenol-A type epoxy resins with various ratios of phenoxy resin employed are shown in Table 1.

The conversions of epoxy groups and the gel contents of the cured epoxy resin are also listed in Table 1. In spite of the content of phenoxy resin, the conversions of epoxy groups are more than 97%. Gel extraction experiment results in 97% for the cured epoxy resin (Sample B-P-0) and decreases gradually with increasing the content of phenoxy resin. When the content of phenoxy resin is subtracted to measure the gel content as phenoxy resin being soluble in tetrahydrofuran solvent, more than 100% gel contents are observed (Sample B-P-20, B-P-30, B-P-40). From this result, it is expected that the linear chains of phenoxy resin are chemically linked to the network chains of epoxy resin and/or long chains of phenoxy resin become unextracted, because of the entanglement with the epoxy resin networks.

Table1. Content of phenoxy resin in epoxy resin and some network properties (System: Bisphenol-A type epoxy resin)

Symbol	Phenoxy resin content (Vol%)	Conversion of epoxy group (%)	Gel content (%)
B-P-0	0	98	97
B-P-10	10	98	99
B-P-20	20	97	105
B-P-30	30	99	109
B-P-40	40	99	110

Figure 1 shows the dynamic mechanical properties of the bisphenol-A type epoxy resin systems cured with DDM. Since the measurement was carried out by using a torsion pendulum in free vibration, the temperature at which shear modulus reduces markedly or at which tanδ becomes maximum is expected to be approximately equal to the glass transition temperature (Tg). All cured systems indicate low-temperature relaxation peaks around -60°C (3-6). The cured epoxy resin with no phenoxy resin shows Tg at 175°C. The systems with phenoxy resin less than 20% (Sample B-P-0,B-P-10 and B-P-20) show broad tanδ peaks. And the temperature of the tanδ peak decreases with increasing the content of phenoxy resin. The system with 40% phenoxy resin (Sample B-P-40) shows two peaks. Small shoulder of tanδ peak at about 100°C is derived from the loss peak of phenoxy resin. It can be deduced from the result that phase separation between the cured epoxy resin and phenoxy resin occurs in this system (Sample B-P-40).

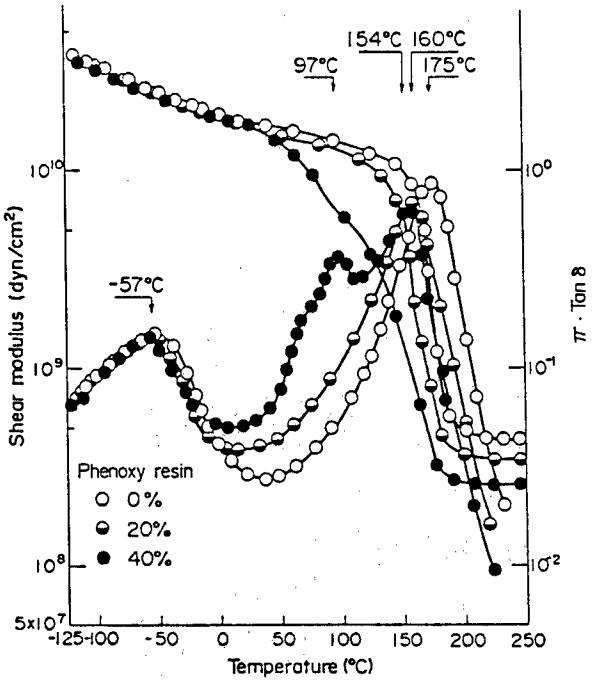

Fig.1. Dynamic mechanical properties of cured bisphenol-A type epoxy resins modified with phenoxy resin.

In general, at the temperature above Tg, the cured epoxy resins are highly crosslinked elastomers. In principle, the crosslinking density (ρ) can be obtained from dynamic mechanical data using the theory of rubberlike elasticity(7) given by:

$$\rho_m = \nu E_R' / 3RT$$

Where ρ_m is the crosslinking density, ν is the specific volume, R is the gas constant, T is the absolute temperature, and E_R' is the equilibrium modulus. It is also possible to obtain the crosslinking density from stoichiometrical equivalent ratio of the components. The value of ρ_c can be caluculated by using the method of Katz and Tobolsky (8-10). The values of the characteristic parameters and the crosslinking densities obtained from two methods are listed in Table 2.

Table 2. Values of characteristic parameter and crosslinking density.(System:Cured bisphenol-A type epoxy resins)

Symbol	Tg (°C) (Tanδ max)	E_R'(dyn/cm²) (Tg+40°C)	ρ_m(mole/cm³)	Z	C(mole/cm³)	ρ_c (mole/cm³) (ZXC)	ϕ_o ($\rho_m - \rho_c$)
B-P-0	175	440×10^8	4.15×10^{-3}	2	1.28×10^{-3}	2.56×10^{-3}	1.44
B-P-10	167	359×10^8	3.00×10^{-3}	2	1.15×10^{-3}	2.30×10^{-3}	1.56
B-P-20	160	351×10^8	2.98×10^{-3}	2	1.02×10^{-3}	2.04×10^{-3}	1.72
B-P-30	156	295×10^8	2.52×10^{-3}	2	8.95×10^{-4}	1.79×10^{-3}	1.65
B-P-40	154	275×10^8	2.36×10^{-3}	2	7.67×10^{-4}	1.53×10^{-3}	1.80

E_R', equilibrium dynamic modulus at Tg+40°C , ρ_m, $E_R'/3RT(T=Tg+40°C)$; Z number of network formed from one molecule of crosslink agent , C, mole number of crosslink agent in unit volume , ρ_c , Z x c ; ϕ_o apparent front factor

The crosslinking densities obtained from two methods are plotted against the content of phenoxy resin as shown in Fig.2. It is noted that the crosslinking density decreases with increasing the content of phenoxy resin. The ratio of f_m/f_c namely, φ_a increases with the increase of phenoxy resin up to 20%. The increase of φ_a suggests that the molecular chains of phenoxy resin react and/or entangle with the network of the molecular chains of the bisphenol-A type epoxy resin.

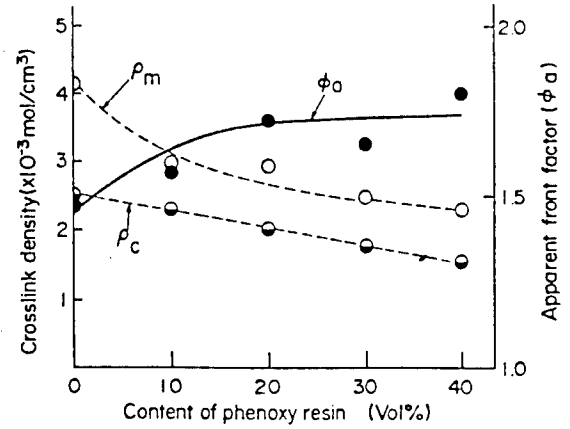

Fig.2. Change of apparent front factor for cured bisphenol-A type epoxy resins modified with phenoxy resin.

With the objective of obtaining information on the morphological structures, scanning electron micrographs of the fractured surface of the systems are taken.

Figure 3 shows the micrographs of the fractured surfaces of sample B-P-20 and sample B-P-40. Relatively smooth fractured surface is seen for the sample B-P-20. On the other hand, some protrusions or particles of about 10um in diameter are seen for the sample B-P-40. From these micrographs, it is concluded that bisphenol-A type epoxy resin and phenoxy resin are miscible each other in the region of less than 20% content of phenoxy resin. In this region, it is deduced that the linear phenoxy resin is interpenetrated and entangled in the network of epoxy resins (semi-IPN). This speculation of the network structure is supported by the results of gel fraction experiment and the measurement of crosslinking density.

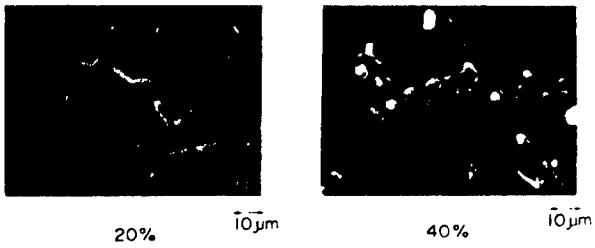

Fig.3. Scanning electron micrographs of fractured surface of cured bisphenol-A type epoxy resins with 20% and 40% of phenoxy resins respectively.

Figure 4 shows the mechanical impact properties of cured epoxy resins. It is obvious from the Fig.4 that force and breakdown energy increase with increasing the content of phenoxy resin up to 30% and then decrease. Data of displacement or elongation also exhibit a peak at about 30%. This phenomenon is explained by considering the morphological change of the systems. The improvement of the mechanical properties can be achieved in homogeneous region. And the decrease of mechanical properties is happened when phase separation occurs.

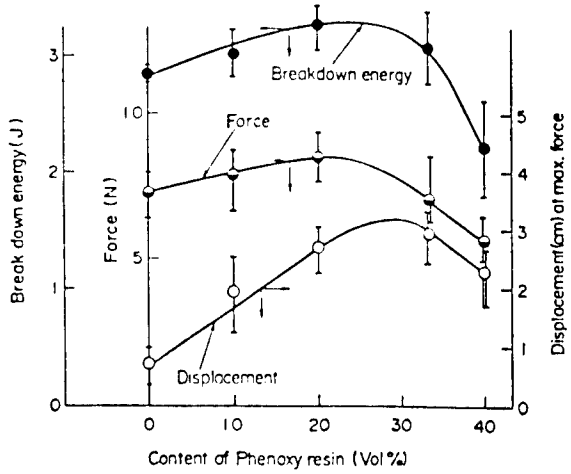

Fig.4. Mechanical impact properties of cured bisphenol-A type epoxy resins modified with phenoxy resin.

(Prove diameter,16mm; Holder diameter,3.8mm; Sample thickness,2mm; Impact speed,5m/s; n=3)

Multi-functional epoxy resin alloy systems

The heat resistant polymer alloy networks were prepared from various contents of phenoxy resin and multi-functional epoxy resins cured with phenol resin.

Table 3. Content of phenoxy resin in epoxy resin and some network properties. (System: Multi-functional epoxy resin)

Symbol	Phenoxy resin content (Vol%)	Conversion of epoxy group (%)	Gel content (%)
M-P-0	0	97	98
M-P-3	3	99	98
M-P-6	6	99	100
M-P-8	8	98	101
M-P-14	14	97	103
M-P-30	30	99	104

Table 3 shows the conversion of epoxy group and gel content of cured resins. The conversion of epoxy group and gel content show the similar tendency as bisphenol-A type epoxy resin systems. In this system, it is also expected that the linear chains of phenoxy resin is chemically linked and/or entangled with the network chains of epoxy resin, although the values of gel content is not large enough compared with bisphenol-A type epoxy resin system.

The result of the dynamic mechanical properties for cured multi-functional epoxy resin shows high glass transition temperature at 220°C. And for the systems containing phenoxy resin more than 8%, the tanδ peaks around 100°C were clearly observed.

In Fig.5 , relaxation strength around 100°C was plotted against the content of phenoxy resin. The relaxation peak is attributed to the motion of main chains of phenoxy resin.

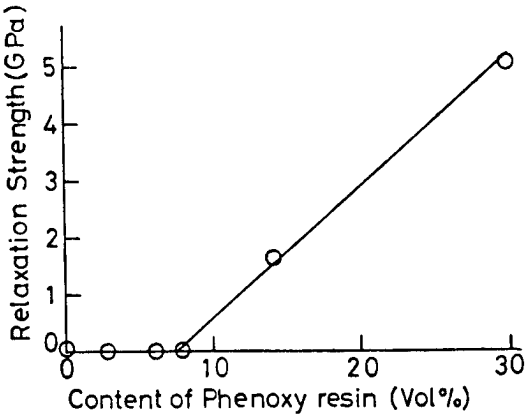

Fig.5. α-Relaxation strength of phenoxy resin for multi-functional epoxy resin systens.

The scanning electron micrographs of the fractured surfaces of the cured multi-functional epoxy resin containing phenoxy resin (Sample M-P-6 and M-P-14) are shown in Fig.6. Phase separation between two resins is not observed in the sample M-P-6, while in 14% phenoxy resin system (Sample M-P-14) phase separation is observed. The particle is about 4μm in diameter. Though the number of particles of phenoxy resin increases, each particle size does not change in the region above 14% of the phenoxy resin content. These results on phase separation phenomena mean that phenoxy resin is more miscible in bisphenol-A type epoxy resin than in multi-functional epoxy resin used here.

On the base of the results on the bisphenol-A type epoxy resin systems, the cured multi-functional epoxy resin systems with the phenoxy resin content less than 6% are also expected to have semi-IPN structure with improved mechanical properties.

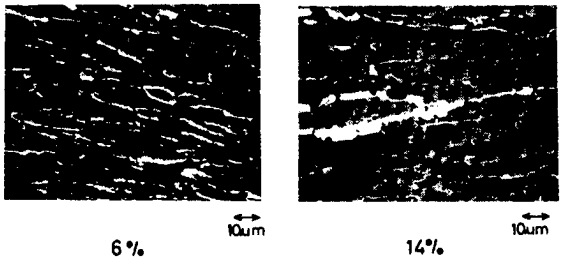

Fig.6. Scanning electron micrographs of fractured surface of cured multi-functional epoxy resins with 6% and 14% of phenoxy resins respectively.

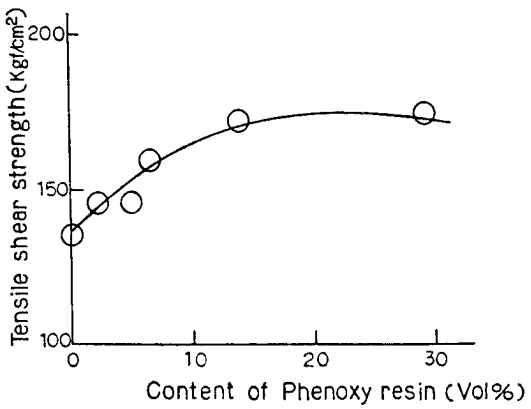

Fig.7. Tensile shear properties of cured multi-functional epoxy resins modified with phenoxy resin.

Figure 7 shows the tensile shear strength of cured multi-functional epoxy resins against the content of phenoxy resin. The tensile shear strength increases gradually until the content of phenoxy resin reaches about 10% and then saturates. In this combination, it is concluded that around 10% of phenoxy resin content is a point to take into consideration for getting base resin systems for PWBs.

CONCLUSION

Polymer alloy systems were studied to prepare new types of laminating resins for PWBs. Two kinds of polymer combinations were employed and characterized.

As a result, we reached the following conclusions.

(1) The similar structural combination of linear, phenoxy resin and thermosetting epoxy resin shows better mechanical properties when the content of the linear polymer is not above 30%. In this region of the alloy system, it is suggested that semi-interpenetrating polymer network structure be formed.

(2) Combination of heat resistant epoxy resin and phenoxy resin has a tendency to decrease the content of phenoxy resin for getting homogeneous structure.

(3) The experimental results of the polymer alloys can be applicable to preparing a new type of heat resistant epoxy resin systems for PWBs.

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THE FACTORS INFLUENCING ENVIRONMENTAL RELIABILITY OF CHIP-ON-GLASS TECHNOLOGY

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ABSTRACT

The chip-on-glass (COG) technique is not yet perfected for practical application, although partial reliability has been confirmed. To examine the practicality of applying this packaging technique to Liquid Crystal Display (LCD) panels, we examined how reliability is affected by different types of glass substrates and sealing resins by using 63%Sn-Pb solder for the bump contacts of a flip-chip.

The results suggested that packaging failure can be reduced even when using 63%Sn-Pb solder bump contacts are used as long as the proper glass substrate is selected. We also confirmed that service life could be prolonged beyond that of a bare chip by selecting the proper resin material. Especially thermal expansion coefficient and longitudinal elastic constant were the most important factors to select the resin material.

INTRODUCTION

LCD panels and driving LSIs have been connected by using such chip-on-board (COB) techniques as the wire-bonding (WB) and the tape-automated-bonding (TAB) method.

In view of the increasing demands for (1) miniaturized packaging capability, (2) high-density multi-pin connection, and (3) lower product costs, greater attention has been given to the chip-on-glass technique using flip-chips on which LSIs are mounted directly on indium-tin-oxide (ITO) film on the LCD panel. This method has already been applied to commercial product, though not extensively. At the same time, the reliability afforded by this chip-on-glass technique has not yet been adequately proven, as compared to the conventional chip-on-board technique method.

It is widely accepted that the reliability of flip-chips can be improved by using a 5%Sn-Pb solder for the bump contacts and lengthening the molten solder to increase the height of bump contacts by special manufacturing process.

However, this height can only be adjusted to a limited extent in actual production, while 5%Sn-Pb solder must be melted at high temperatures exceeding 300°C. Thus, there is anxiety among researchers that the reliability of such components as the glass substrate (= LCD panel) may be adversely affected.

This paper discusses how we evaluated the reliability of chip-on-glass structures when the 63%Sn-Pb solder is used for the bump contacts and the solder is molten at a low temperature. Because these factors directly affect reliability, we selected the most appropriate glass substrate material with ITO film and the sealing resin. The connection resistance and the shear strength are used as the evaluation items. Based on the obtained results, we also studied mechanisms to improve reliability from a theoretical standpoint.

MATERIALS AND METHODS

1) Specimens for COG technique

Figure 1 shows the schematic drawing (see (a)) and cross section of a glass substrate specimen (bonded to a silicon chip) facing downward (see (b)). The silicon chip (5.3 x 6.3 x 0.3t [mm]) has bump contacts consisting of 63%Sn-Pb solder plated around the chip's periphery. The electrodes next to the bump contacts are shorted using Al pattern wiring to be aligned in a line. There are 75 bump electrodes, each of which is 60 μm high before solder-melting.

To simulate the LCD panel film, Cr-Cu films were evaporated on ITO film on the glass substrate (26 x 24 x 1.1t [mm]). The film's circuit is arranged so that the connection resistance of the bonded chip can be measured in series. Each connecting area of the solder bump contacts is formed on a circular pad (50μm in diameter) with a minimum pad pitch of 190μm.

Finally, liquid resin was filled in the gap between the chip and the glass substrate.

2) Evaluating Reliability Through Thermal-Shock Tests

We evaluated reliability through thermal-shock tests by observing environmental resistance. The conditions for these thermal-shock tests were: (A) 120°C/-40°C,1 hr./cycle or (B) 80°C/-40°C,1 hr./cycle. Changes in resistance values were used as the evaluation criteria. The resistance value refers to the value when the chip and substrate pads are aligned in series through 75 pads. In this way, any failure in part of the connecting area will cause a change in resistance. If the resistance value becomes doubles the initial value, it is considered a rejected value (failure).

3) Theoretical Analysis

When connecting materials whose thermal expansion coefficients or longitudinal elastic constants were different, we found that such differences caused stress and fractures to occur where maximum stress was measured. For the structures using four types of sealing resins, we used a finite element method (FEM) model to analyze the thermal stress distribution (in the solder bump contacts) that occurred due to change between room temperature (where strain was assumed to be zero) and -40°C (lowest temperature used in the thermal-shock tests).

EXPERIMENTS

1) Selecting a Glass Substrate Material

In conventional COB technique we know that reliability is greatly affected by the difference in thermal expansion coefficients between the chip and substrate. To verify this fact, we used barium-borosilicate glass ($=4.6 \times 10^{-6}$ /°C), which is commonly used for LCD panels, and inexpensive soda-lime glass ($=9.0 \times 10^{-6}$ /°C) that is commercially available. We compared the differences in their resistance and connecting strength (actual shear strength) values during 100-cycle thermal-shock tests (with the condition A).

2) Adhesion strength

Imperfect adhesion between the glass and the film causes some local failures such as cracks and film lift at the early stage of the cyclic thermal-shock test. Therefore the adhesion strength between the glass and the film was measured and evaluated with the peel test.

3) Sealing Resin Material

In COB technology, sealing a bare chip with a sealing resin is an essentially basic technique used to improve reliability. This is because the service life of a sealed chip is not always longer than that of a bare chip. In consideration of this point, we evaluated how reliability was improved by using four types of resins (see Table 1) selected in view of the desired specifications. We made our evaluation based on how resistance values varied according to the number of thermal-shock test cycles (condition B).

RESULTS AND DISCUSSION

1) Thermal-Shock Tests on Substrates with Different Thermal Expansion Coefficients

Two types of substrates were evaluated in the bare-chip state. Figure 2 shows the evaluation results. By using the cumulative failure rates for comparison purposes, a zero failure rate in 100 cycles was obtained in barium-borosilicate glass having a low thermal expansion coefficient, while 100 cycles were not possible in soda-lime glass having a high thermal expansion coefficient.

Comparing changes in the average shear strength before and after the thermal-shock tests, we discovered the shear strength was about triple in the soda-lime glass substrate than in the barium-borosilicate glass, although there was a decrease in strength in both substrates. The results indicate that reliability may be improved by using a substrate with a low thermal expansion coefficient, especially when the thermal expansion coefficient of the substrate is close to that of the silicon chip. Barium-borosilicate glass was used in the following tests to evaluate reliability.

2) Effect of initial adhesion strength

We thought that a initial failure was caused by lower actual adhesion strength than design value between films and substrate, or by larger warp of substrate. Thus, we measured adhesion strength.

Figure 3 shows the measurement results. As the figure indicates, the adhesion strength of each point of substrate widely distributed from specified strength.

It is necessary for the bump connections to reinforce structure with a resin. Because adhesion strength between films and the glass was not enough to unify, and adhesion strength between solder bumps and the glass substrate decreased by thermal-shock cycles (as shown in Figure 2).

3) Thermal-Shock Tests on Sealing Resin Specimens with Different Characteristics

We evaluated by thermal-shock tests on four types of coating resins having different thermal expansion coefficients and longitudinal elastic constants. Figure 4 shows the test results (using bare chip reliability as the comparison criteria).

The results show that the sealing process can prolong interconnecting life from the approximate 300 cycles obtained by unsealed bare chips. For the epoxy-resin coating shown in the figure, failure begins to occur at about 300 cycles (although reliability is still higher than that of the bare chips). We also found that by lowering the thermal expansion coefficient by adding a filler, we could surpass 500 cycles. And also the case when using a silicon resin whose thermal expansion coefficient was one digit higher than that of epoxy resin (provided that the silicone resin is soft and in fluid-gel state).

Consequently, it appears possible to improve reliability by minimizing the difference ($\Delta\alpha$) between thermal expansion coefficients of the coating resin and solder, or by using a fluid coating resin having a small longitudinal elastic constant. We think that a rubber silicon did not have coldproof (at -40°C) ,and for that reason it caused the failure.

4) Theoretical Analysis

The failure of resin-inserted flip-chip may be primarily caused by a crack forming near the interface between the bump contacts and glass substrate, and extending into the glass from the outside toward the inside. And resin stress is sheared off the glass near chip-edge. We noticed that cracks initially form on the substrate, then move directly from the periphery of the chip toward the center of the chip. Therefore, such cracking appears to be caused by differences in the thermal contraction force that occurs from the heating cycle toward the cooling cycle of the thermal-shock tests. (see Figure 5 (a))

Note that in the FEM analysis results, shown in Figure 5 (b), the maximum stress also occurs at the same position.

CONCLUSION

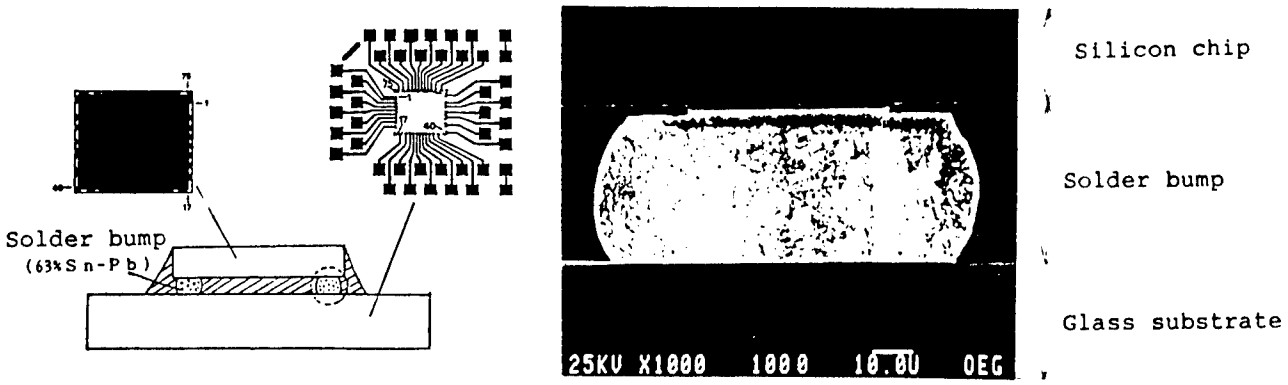
We reached the following conclusions regarding a COG structure:

(1) A glass substrate with a thermal expansion coefficient approximating that of the chip must be selected.

(2) To ensure reliability, the initial adhesion strength between films and the glass must be increase, and its strength should not disperse.

(3) A sealing resin having a low thermal expansion coefficient or a low longitudinal elastic constant must be selected according to intended application.

(4) Failure point of the experimental sample sealed resin was coincident with the maximum stress point revealed through FEM analysis.



(a) COG structure (b) Solder bump interconnection

Fig.1 Experimental Sample

Table 1 Specifications of the coating resin

Sample No.	A	B	C	D	E
1.Resin type	Epoxy	Epoxy	Silicone	Silicone	
2.Color	Black	Black	Transparent	Semi-transparent	
3.Composition	one	one	two	two	
4.T.E.C (*) α[x10^{-6}/°C]	60	20	300	300	
5.Note	Low stress	Filer	Gel	Rubber	Non-sealing

(*)T.E.C:Thermal Expansion Coefficient

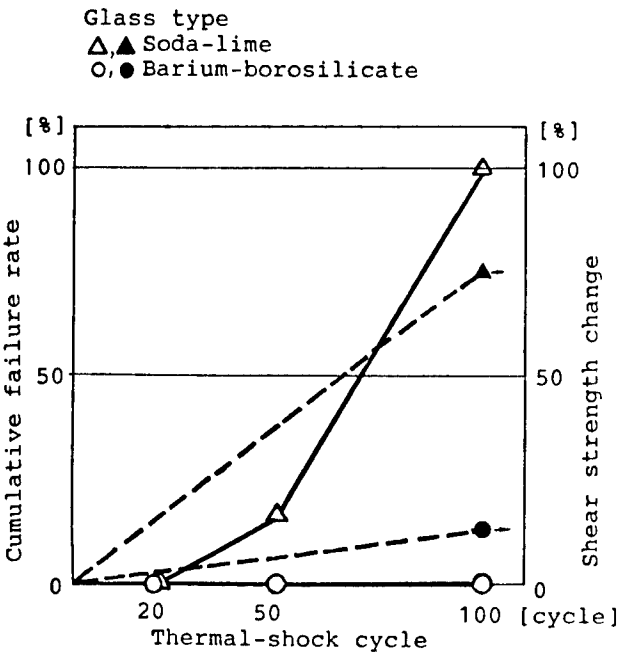


Fig.2 Cumulative failure rate and shear strength change of different glass substrate material

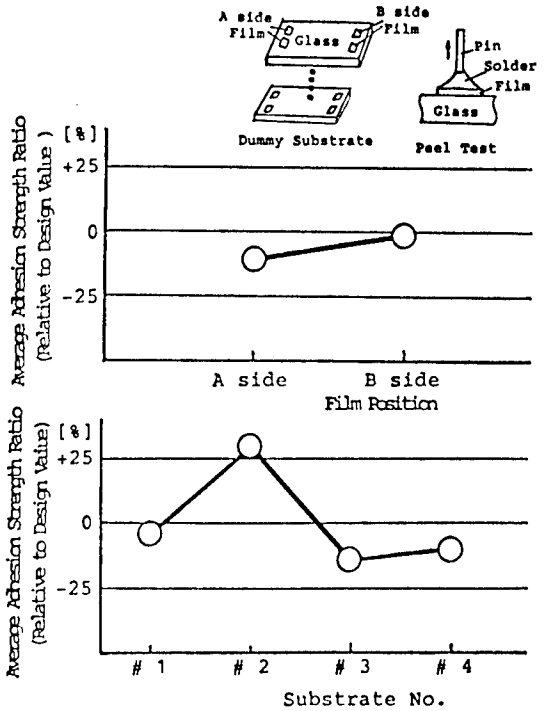


Fig.3 Result of adhesion strength between the glass and the film measurement with peel test

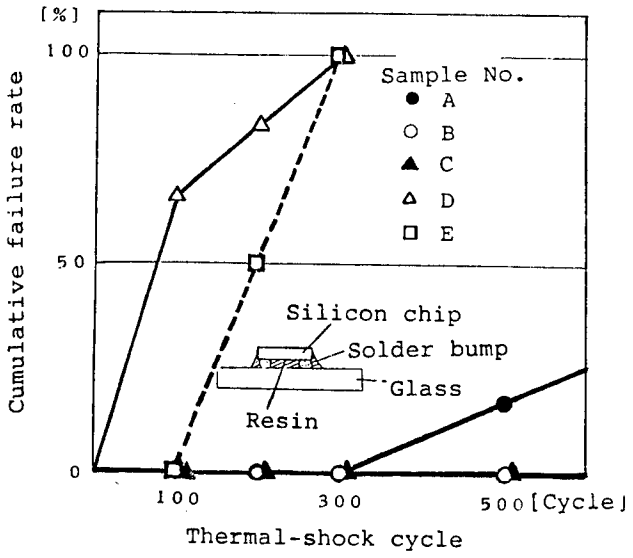


Fig.4 Effect of each type of resin sealing evaluated by thermal shock test

Table 2 Phisical constants for analysis

	Thermal Expansion Coefficient α[x10^{-6}/°C]	Longitudinal Elastic Constant E[kgf/mm^2]	Poisson Ratio ν
Si chip	2.4	17000	0.066
Solder	24.5	1550	0.4
Glass	4.6	6900	0.28
Resin A	60	250	0.076

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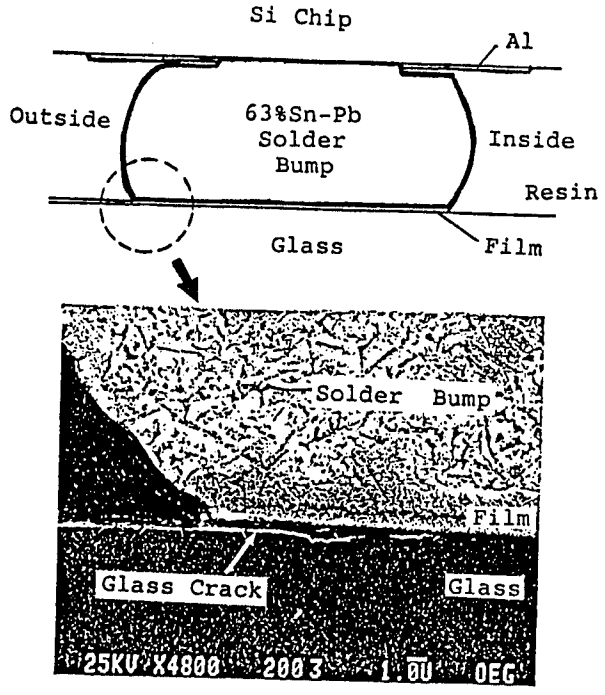
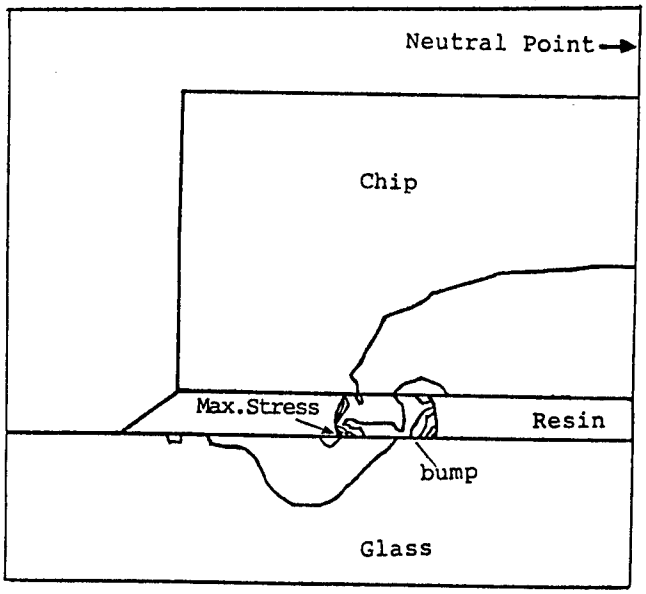


(a) Failure mode



(b) Thermal stress distribution

Fig.5 Relationship between experimental result and FEM analysis

A FALSE ALARM REDUCTION METHOD FOR PWB PATTERN INSPECTION SYSTEM

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Abstracts

Among optical pattern inspection methods for PWB's (Printed Wiring Boards), a feature extraction method achieves higher throughput than a design data comparison method. On the other hand, it can not avoid false alarms completely. This paper proposes an "Error Code Chain" method to reduce these false alarms.

A hierarchical defect analysis technique is employed combining the feature extraction method and the Error Code Chain method. It discriminates between fatal defects and false alarms taking global features into account.

This method has been applied to the Pattern Inspection (PI) system[1], and it has performed both false alarm reduction and video-rate processing.

1. Introduction

The feature extraction method is widely used for optical pattern inspection for PWB's. It judges defects by features extracted from local patterns using no reference data for comparison. High processing rate can be achieved by hardware implementation.

Several feature extraction operators have been proposed as shown in Fig.1[1][2]. Since each operator extracts local features in the window specified by its size, global features are often ignored. Thus a normal pattern can be judged as a fatal defect, that is, a false alarm can be occurred. Fig.2 shows some examples. False alarms are often found at round corners called "tear drops" or at SMD lands.

Design data comparison method has been adopted to reduce false alarms[3]. However design data should be prepared for each board type, and precise alignment is indispensable.

Global feature extraction is effective to reduce false alarms. Extension of operator size can be applied for that purpose, but it requires larger hardware size and longer processing time.

In this paper, the "Error Code Chain" method is proposed to reduce false alarms without decrease in throughput.

2. Goals

The Error Code Chain method is aimed at false alarm reduction with following three features.

(1) Hierarchical analysis

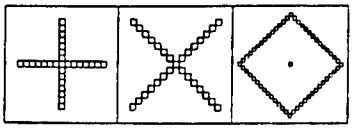
The Error Code Chain process receives local features from the feature extraction process. By analyzing a series of local features, global features can be obtained.

(2) Pipeline architecture

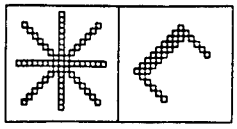
Hierarchical two processes can be carried out in pipeline architecture, and video-rate processing can be realized.

(3) Applicability

The generalized concept allows this method to be applied to most of feature extraction operators for PWB inspection.



PI System [1]



FVIS-350 [2]

Fig.1 Feature Extraction Operators

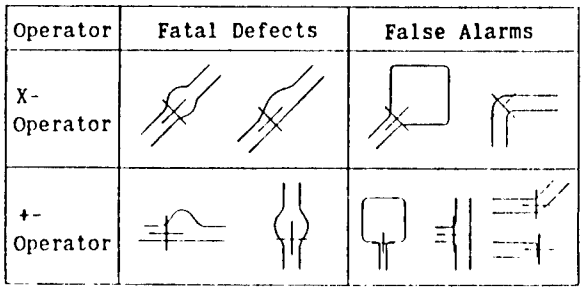


Fig.2 Fatal Defects and False Alarms in PI System

3. Algorithm

Fig.3 illustrates the hierarchical defect analysis with the Error Code Chain method. It works as if it employed a large sized operator never realized in conventional architectures. Thus, both local patterns and global patterns are taken into account to reduce false alarms.

Hierarchical processes and its hardware configuration are as follows.

3.1 Feature Extraction Process

In the feature extraction process, the two dimensional input image is compressed to a linear code chain. Scanning on a PWB, the operators calculate the features for each pixel. An error code is generated corresponding to the defect type on the pixel. In our method, it is regarded as a defect candidate. The defect detection results in this process may contain some false alarms to catch all fatal defects.

3.2 Error Code Chain Process

The Error Code Chain process analyzes a series of the error codes (error code chain) generated by the feature extraction process. Fatal defects can be recognized by matching them with fatal defect code chains.

The error code chain makes it possible to analyze global features as well as local features. Since the error code chain lies in a linear direction, matching operation can be implemented on a simple hardware to realize video-rate processing easily.

3.3 Configuration

Fig.4 shows the hardware configuration to implement the Error Code Chain process. In a pipeline architecture, video-rate processing is realized.

The Error Code Chain hardware consists of a shift register and a fatal defect decision table. The shift register receives error codes from the feature extraction hardware and holds an error code chain. This error code chain is compared with fatal defect codes stored in the table.

4. Application to PI system

4.1 PI system

The Error Code Chain method has been applied to the PI system[1]. This system employs +-operator, X-operator, and rectangle operator in the feature extraction process (Fig.1).

As shown in Fig.2, the feature extraction method introduced some false alarms of fat line at connectors to land, corners and branches of line.

An error code consists of defect candidate codes and online codes in 8 directions. An online code shows the directions of continuous copper patterns in the window. Global features are caught by analyzing online codes. For example, a line in the scanning direction can be found by a series of online codes in horizontal direction. A vertical line can be found by a series of vertical online codes.

4.2 Target Defect and its Analysis

A fat line false alarm is one of the most troublesome false alarms for the PI system. Fat line has been chosen as the target defect to apply the Error Code Chain method.

Fig.5 illustrates fat line false alarms and fatal defects. Each of them is shown in three cases of line patterns; oblique line, horizontal line, and vertical line. In every case, the error code chain is realized in horizontal direction (rectangular area in Fig.5). When a fat line code appears at the center in the chain, following conditions are checked according to the online codes at the central pixel.

(1) Oblique online code

The horizontal online code is used to catch the global pattern. Existence of a bending line corner is the key to discriminate false alarms. If a horizontal online code is found at either end, the fat line

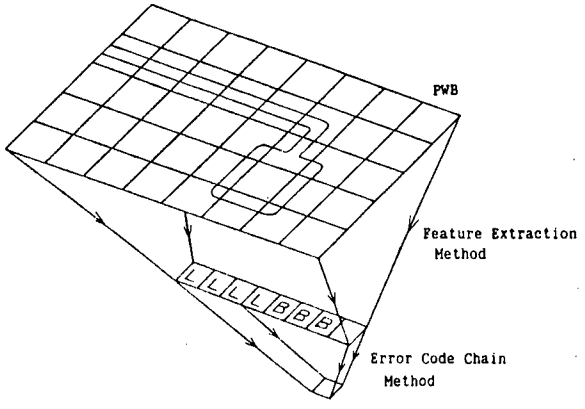


Fig.3 Hierarchical Defect Analysis

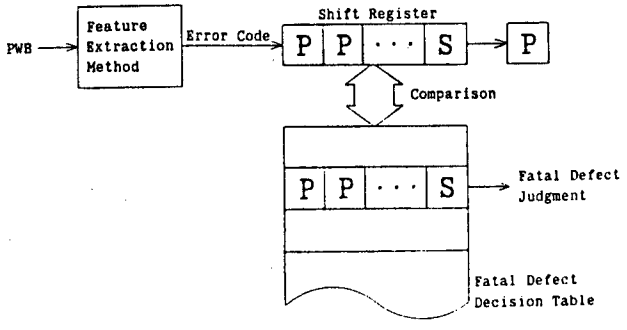


Fig.4 Configuration of Error Code Chain Method

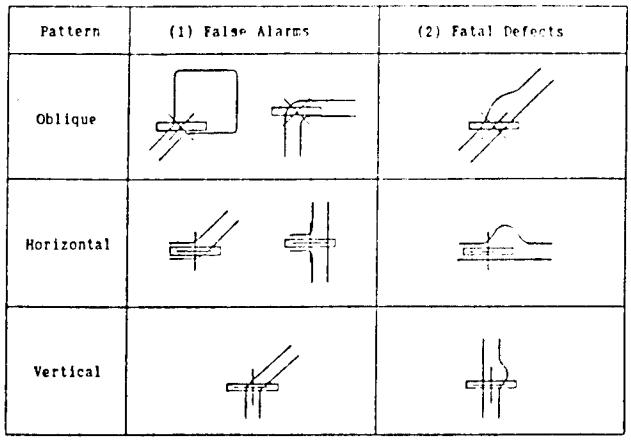


Fig.5 False Alarms with Fat Line Code

code is rejected as a false alarm at a bending line corner. Otherwise it is judged for a fatal defect.

(2) Horizontal online code

False alarms can be found at a line corner, a branch, and a connector to a land. They are discriminated by checking online codes at the ends of the chain. If horizontal online code is shown at the both ends and no vertical online code is found, the line is assumed to have a fat line fatal defect. Otherwise the fat line code is rejected as a false alarm.

(3) Vertical online code

Distribution of vertical online codes is examined to reject fat line false alarms at a bending line corner, a branch, and a land. If the length of vertical online codes matches to the width of fat line, the fat code shows a fatal defect. Otherwise it is rejected.

Thus, false alarms is discriminated against fat line fatal defects.

4.3 Hardware Configuration

Fig.6 shows the hardware configuration of the Error Code Chain process applied to the PI system. It is composed of the error code chain register and two fatal defect decision tables. Each table is used for vertical line pattern inspection, and horizontal or oblique one. The image in a window is encoded to a code including fat line code and online codes. It is examined in the Error Code Chain process.

When a fat line code appears at the center of the chain, fatal defect analysis is made according to the line pattern direction in the window.

(1) Horizontal or oblique line

Online codes on the center and two points on both sides of the chain are used for fatal defect analysis. The locations of the two points on both sides can be changed according to the design rule.

(2) Vertical line

Oblique online codes at the center and length of vertical online codes are used. The length predicts the width of a vertical line pattern if the pixel is located on it. The oblique online code is used to check bending corner on a line pattern.

In both cases, the fatal defect decision condition is stored in ROM's. Their address bit widths are 16. Their contents are programmable according to the design rule.

4.4 Performance

The Error Code Chain method has been evaluated by simulation on a image processing computer system. Following points have been examined.

(1) Fatal defect detection ratio
(2) False alarm reduction ratio
(3) Reduced false alarms and remained ones

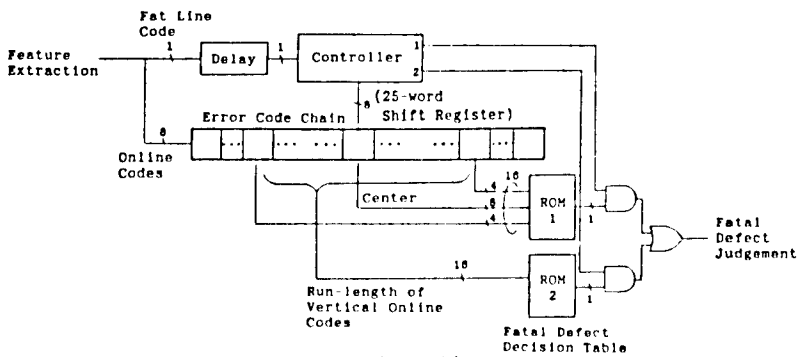


Fig.6 Configuration

The Error Code Chain has 25 pixel length in the simulation.

Two kinds of sample patterns have been applied; one includes fatal defect patterns of fat lines, and the other contains no fatal defect and caused false alarms as fat lines. They have been extracted from several kinds of PWB's and the number of them exceeds 600. Table 1 shows fatal defect detection ratio and false alarm reduction ratio. Number of samples applied to each test is shown in parentheses.

Fatal defects have been detected at 100 % for every line direction. False alarm reduction rates on horizontal and oblique lines are respectively 95 % and 92%. However, the false alarm reduction ratio on vertical lines has been limited to 47 %.

The Error Code Chain method has reduced false alarms shown in Fig.5 by capturing global features of line patterns. As to the connector of vertical line to a land (Fig.2), this method has failed to reject a false alarm because the available global features in vertical direction is now limited by the window size. It can be rejected with a vertical code chain.

As a result of logic simulation for the circuit, the pipeline organization of the Error Code Chain has been confirmed to realize the video-rate processing.

Table 1 Fatal Defect Detection Ratio and False Alarm Reduction Ratio

Pattern	Fatal Defect Detection Ratio	False Alarm Reduction Ratio
Vertical Line	100% (66)	47% (153)
Horizontal Line	100% (66)	95% (160)
Oblique Line	100% (132)	92% (72)

5. Conclusion

This paper has proposed the Error Code Chain method to reduce false alarms for PWB pattern inspection system. Local features extracted from the image are examined in a linear chain to capture global features. The hierarchical defect analysis concept is the key to reduce false alarms taking both local and global features into account.

This method has been applied to the PI system and evaluated in point of fatal defect detection ratio and false alarm reduction ratio. It has been demonstrated that the Error Code Chain method misses no fatal defects and eliminates most of false alarms from the feature extraction process.

In the future work, the Error Code Chain method will be applied for other kinds of false alarms, such as a SMD land.

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